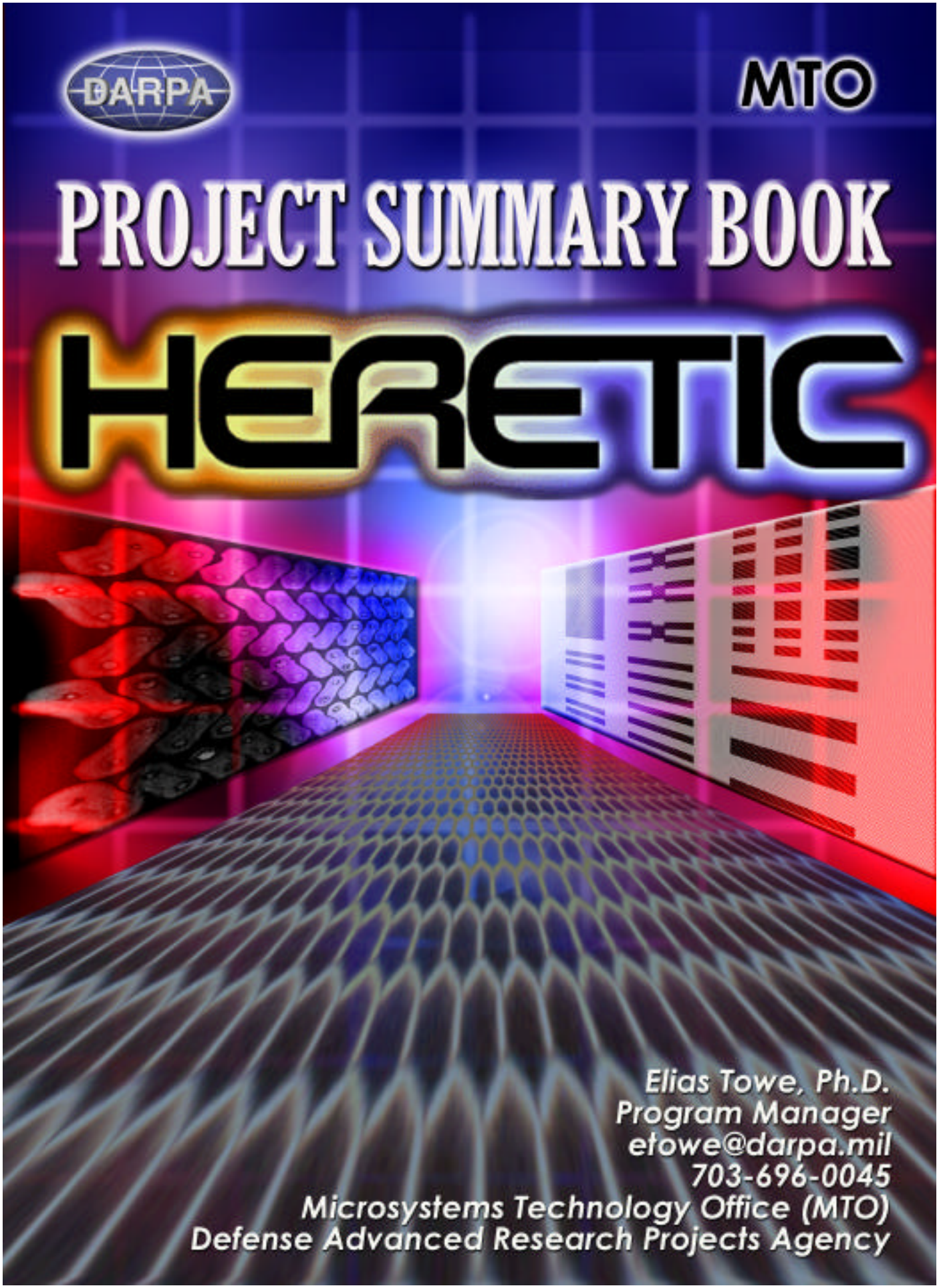
DARPA
MTO
PROJECT SUMMARY BOOK
HERETIC
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Microsystems Technology Office (MTO)
Defense Advanced Research Projects Agency

FOREWORD

This booklet contains a summary compilation of the projects supported under the DARPA HERETIC Program. The document is intended to serve as a quick guide to the objectives, accomplishments, and future milestones of the projects in the program.

Details of the individual projects can be obtained by contacting the principal investigator listed as the point-of-contact for each project. Please note that this document does not replace the semi-annual reports prepared by the investigators. If you need general information about the HERETIC Program, please feel free to contact me.

I want to thank the principal investigators for their efforts in striving to achieve the objectives of the program as enunciated in the vision. I also want to acknowledge the support and assistance of Ms. Claire T. Heller who compiled the materials in the document and prepared the booklet.

Elias Towe, Ph.D.
Program Manager
Microsystems Technology Office
Arlington, Virginia
June, 2000

Table of Contents

THE HERETIC OVERVIEW

The main objective of the HERETIC Program is to develop solid-state and micro-fluidic heat removal devices that are integrable with dense, high-performance electronics and photonics. These devices are envisioned to be capable of short-circuiting the thermal resistance between heat sources and the thermal sinks; they should also lead to a reduction in overall system volume and weight. It is expected that devices will be designed for high efficiency operation (in terms of work done to remove a unit of heat from a hot junction).

Traditional thermal management in many electronic and optoelectronic systems is generally relegated to the end of the process sequence in the packaging of the systems. For non-critical applications, where the systems are used in relatively benign environments, this approach is cost-effective and has worked well. This *ad hoc* method of thermal management is inadequate and the need for new or novel approaches becomes evident in certain situations. These situations may be: where the system package must be small and compact; where the density of high-performance, high-power chips on a board is high; where the thermal load is not fixed, but changes with time; or where the environment is thermally harsh.

In conventional thermal management, heat removal or cooling is typically addressed hierarchically. The first level of the hierarchy is at the system level, the second is at the board level, and the third is at the chip-package level. As a typical example, consider the following case: at the system (box) level, global air circulation may be effected by a fan which blows over boards that comprise the system; at the board level, the chips may be mounted on a board that allows the circulation of a coolant through it; and, at the chip-package level, the package (containing a telecommunications laser chip or a special processor chip, for example) could be cooled directly by a thermoelectric cooler. The focus of this program is at the chip and board levels.

The program aims to exploit recent developments in micro-fabrication technologies (such as micro-machining) and advances in heterogeneous materials integration in microelectronics to develop novel heat removal devices that are integrable with electronics and optoelectronics. There are four areas of interest: (1) core technology development, (2) integration and packaging, (3) modeling and simulation, and (4) demonstrations.

In the core technology area, we seek to develop novel heat removal or cooling devices in electronics and optoelectronics. The cooling devices must be integrable with electronic or optoelectronic devices fabricated from common semiconductor materials. Of particular interest are heterostructure integrated thermionic (HIT) or thermoelectric devices, and phase-change heat removal devices. Other devices of interest include micro-machined synthetic jets or nozzles and channels that can act as micro-circulators of air or fluids in individual chip-packages; these micro-coolers, however, must be integrated with chip packages. Micro-machined devices may also include thermionic emitters that

exhibit credible cooling when integrated with active electronic or optoelectronic devices that generate waste heat.

In the integration area, we will develop technologies to integrate the devices developed in the program with active electronics or optoelectronics. This involves the integration of large arrays (when necessary) of HIT coolers, synthetic micro-jets, micro-fluidic devices, or other cooling devices with control circuitry to effectively manage heat removal from electronic or optoelectronic chips or sub-systems. One of the key and important features of the integration process is that the heat removal process be active, on demand, and localizable wherever it is needed. The integration and packaging process should be compatible with standard microelectronic processes.

Modeling and simulation are an important and integral part of the program. Modeling should be carried out to quantify the efficiency of the new devices; it should be used as a guide to determine the best placement of cooling devices within electronic or optoelectronic packages, or on active devices to obtain optimal performance.

The technology demonstrations in this program aim at using the novel cooling devices in real applications. This task is envisioned to be a set of demonstrations that show heat-removal capacities equal to or better than the best conventional solution to specific problems in a more compact, and adaptable form. The aim of the demonstrations is to clearly show how the new thermal management schemes couple with cooling at the system level, and that the new approach brings a significant level of improvement in overall thermal management and efficiency.

The stressing demonstrations in the program will use military electronic and optoelectronic systems as test-beds. One of the goals of the demonstrations is to develop clear and quantifiable metrics for assessing the cooling capabilities of the new devices and systems.

Performer: CFD Research Corporation

Hierarchical CAD Tools and Thermoelectric-Fluidic Devices for Active Refrigeration and Control of Thermo-Integrated Circuits (ARCTIC)

PI: Dr. Andrzej Przekwas (256) 726-4815

Other Team Members:

Marlow Industries, Dr. Hylan Lyon
Irvine Sensors, Dr. Volkan Ozguz
UCLA, Professor Gang Chen

Agent: ONR

Dr. Colin Wood (703) 696-4218

Project Goals

The overall objective of this project is to develop configurable, multi-disciplinary, hierarchical simulation tools for design of hybrid thermoelectric-fluidic actively controlled heat removal devices and their assemblies in computing/communication systems; design, fabrication, and testing of integrated thermoelectric-fluidic refrigeration plates, and demonstrate them on thermal management of VCSEL arrays and on 3D stacked wafer ICs ("sugar cubes"); and to provide computational software and support to all other HERETIC teams.

Approach

A combined technical approach for multi-disciplinary computational technology, hierarchical software architecture, new refrigeration device, and support to all other HERETIC teams

Accomplished Milestones

- Release of CFD-MicroMESH V1.0 for 3D automated geometrical modeling and meshing of fluidic, thermal, and electric circuits
- Implemented 2D/3D DD electric solver for semiconductor devices
- Designed an innovative concept of impinging microchannels for enhanced heat removal and precise control of spatial temperature profiles
- Designed a test bed for evaluating microchannel and thermoelectric cooling of Irvine Sensors' 3D high power density packages
- Provided software support of HERETIC teams

Near-Term Milestones

- Development of 1D/2D/3D Thermoelectric device models
- Implementation of two phase with phase change models for refrigeration cooling of integrated circuits
- Experimental evaluation of the concept of impinging microchannels and thermoelectric coolers for 3D packages
- Design of a meso scale system for cooling laptop computers
- Continued software support of HERETIC teams

Long-Term Milestones

- Development of Quantum-Well TEC Modeling in CFD-ACE+
- Definition of Formats and Material Properties for TEC CAD Tool
- Compact Cooling Designs for 3D Stacked ICs and Photonics Interconnect
- Mixed Dimensionality CAD for 3D Device and 1D Loop
- Demonstration of Spot Cooling System
- Continued software support of HERETIC teams

Demonstration Activity

We will demonstrate CFD-microMESH for automated model setup of electronic and optoelectronic devices and packages

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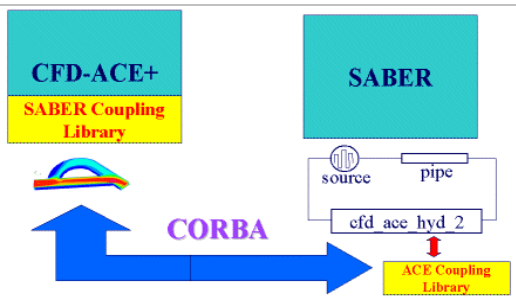
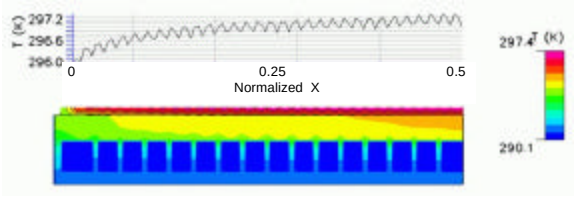
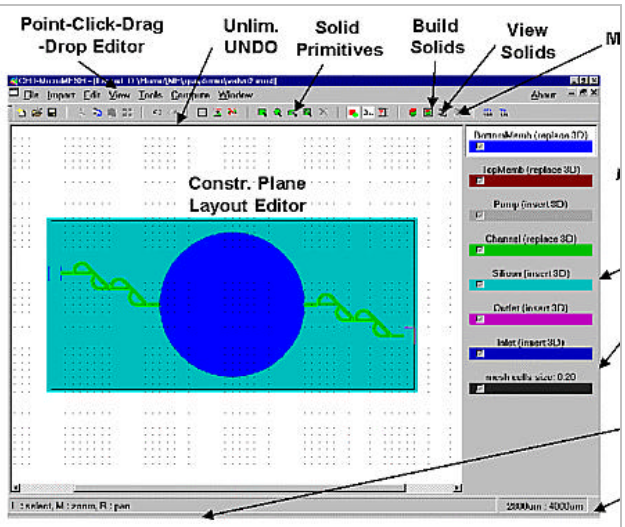


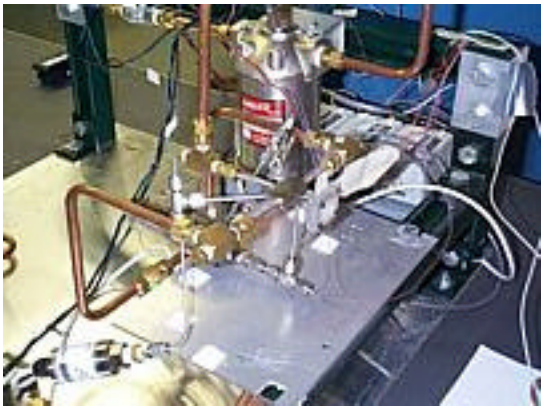
Implementation of SABER - ACE+ Coupling



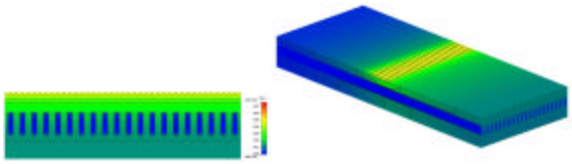
Thermal Fields for Diamond Heat Sink with Embedded Microchannels (Half Domain)



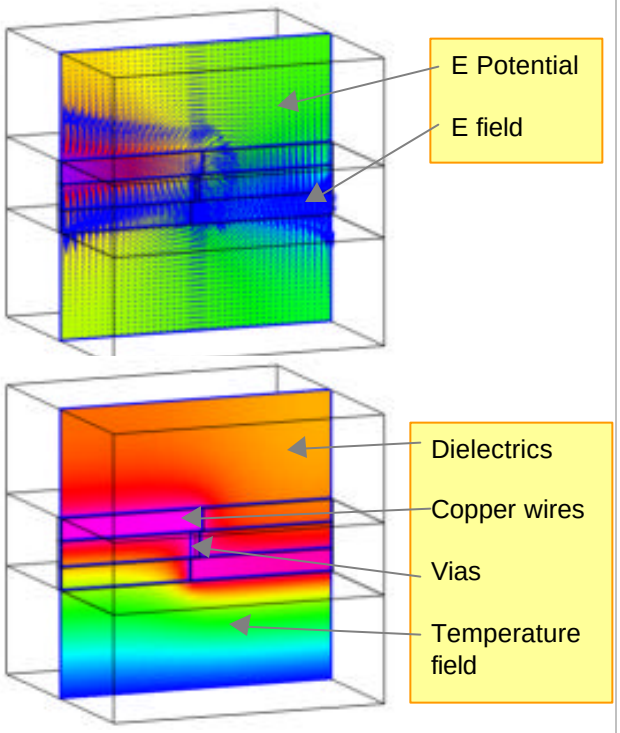
CFD-Micromesh For Automated Model Setup Of IC Interconnects, Electronic/Optoelectronic Modules, And Fluidic Devices



A Compact Fluidic System For Thermal Testing Of Thermoelectric Fluidic Coolers For 3D Packages, And Laser Diode Arrays



Thermal Map Of The Si Microchannel Cooling System Of Laser Arrays Using 3d Thermal/Flow Model



Thermal And Electric Models Of Stanford Interconnects

Performer: Carnegie Mellon University

EDIFICE: Embedded Droplet Impingement for Integrated Cooling of Electronics (EDIFICE)

PI: Professor Cristina Amon (412) 268-4343

PI: Professor Jayathi Murthy (412) 268-3677

Other Team Members:

University of Pittsburgh, Professor Mingking Chyu
Carnegie Mellon University, Professors Kaigham Gabriel, Prashant Kumta, Shi-Chune Yao
IBM, Dr. Sukhvinder Kang
Aavid Thermal Technologies, Dr. Vivek Mansingh
Raytheon, Dr. Donald Price

Agent: ONR

Dr. Colin E. Wood (703) 696-4218

Project Goals

The objective of this project is to design and build an integrated droplet impingement cooling device called EDIFICE (Embedded Droplet Impingement for Integrated Cooling of Electronics) for removing heat fluxes from electronics packages in the range of 50-100W/sq.cm. EDIFICE employs the latent heat of vaporization of dielectric fluids to achieve very high heat removal rates. It will contain built-in software on the chip to provide on-demand cooling. Control of droplet sizes, impingement frequencies and impingement locations is based on on-chip sensing of temperature, thermal gradients and film thickness. EDIFICE will be itegrated into the chip package and will be fabricated using micro-manufacturing technologies. Droplets will be created thorugh a number of novel mechanisms including micro-nozzles, swirlers and vibrating PZT transducers. The development of EDIFICE will involve modeling, numerical simulation, and physical experimentation on test beds to quantify device performance, create software to support product design, optimization and planning, and to create EDIFICE compact models for integration into system-level thermal design. At the system level, air-side cooling designs suitable for commercial portables and desktops as well as completely sealed designs using phase change materials (PCMs) will be developed. EDIFICE will be demonstrated and evaluated for commercial and DOD-related electronics cooling applications.

Approach

- Create efficient spray devices by tailoring jet instability mechanisms using micromanufactured turbulators and other geometric features, or by actuation
- Employ Deep RIE and CMU-CMOS MEMs for nozzle fabrication, sensing and surface micromachining
- Test these devices in an experimental test bed and pick the best design
- Incorporate EDIFICE into the chip package and test at the system level
- Support the design and optimization of EDIFICE with simulation at the device and system levels

Accomplished Milestones

- A variety of nozzle designs have been micromanufactured in silicon for different opening shapes and sizes
- Valves for control of flow through nozzles have been micromanufactured
- A test-bed has been constructed and instrumented for testing the first generation of EDIFICE designs
- Testing of nozzles has begun and flow visualization of the performance of different nozzle designs is being performed
- Design of chip surface enhancement geometries has been completed. These are required to create thin films and to promote boiling.
- Computational fluid dynamics (CFD) models for impingement physics have been created and computations have been made of the thermal performance of various impingement scenarios
- CFD models have been created and simulations performed for the air-side cooling mechanisms to understand the heat transfer limitations posed by the air side

Near-Term Milestones

- Complete testing and identification of promising nozzle designs
- Complete fabrication of surface enhancements
- Test nozzle and enhancements together
- Extend and refine CFD models at device and system level

Long-Term Milestones

- Design system-level cooling, including system-level heat sinks, condensers, pumps and heat storage units
- Create mock-up of EDIFICE in closed-loop system
- Create lower-dimensional compact models for system simulation; iterate between design and simulation
- Complete final fabrication of EDIFICE and integrate into system
- Demonstrate heat removal capacity on chosen system

Demonstration Activity

We will develop a proof-of-concept demonstration of EDIFICE in a closed-loop system and quantify its heat removal capacity.

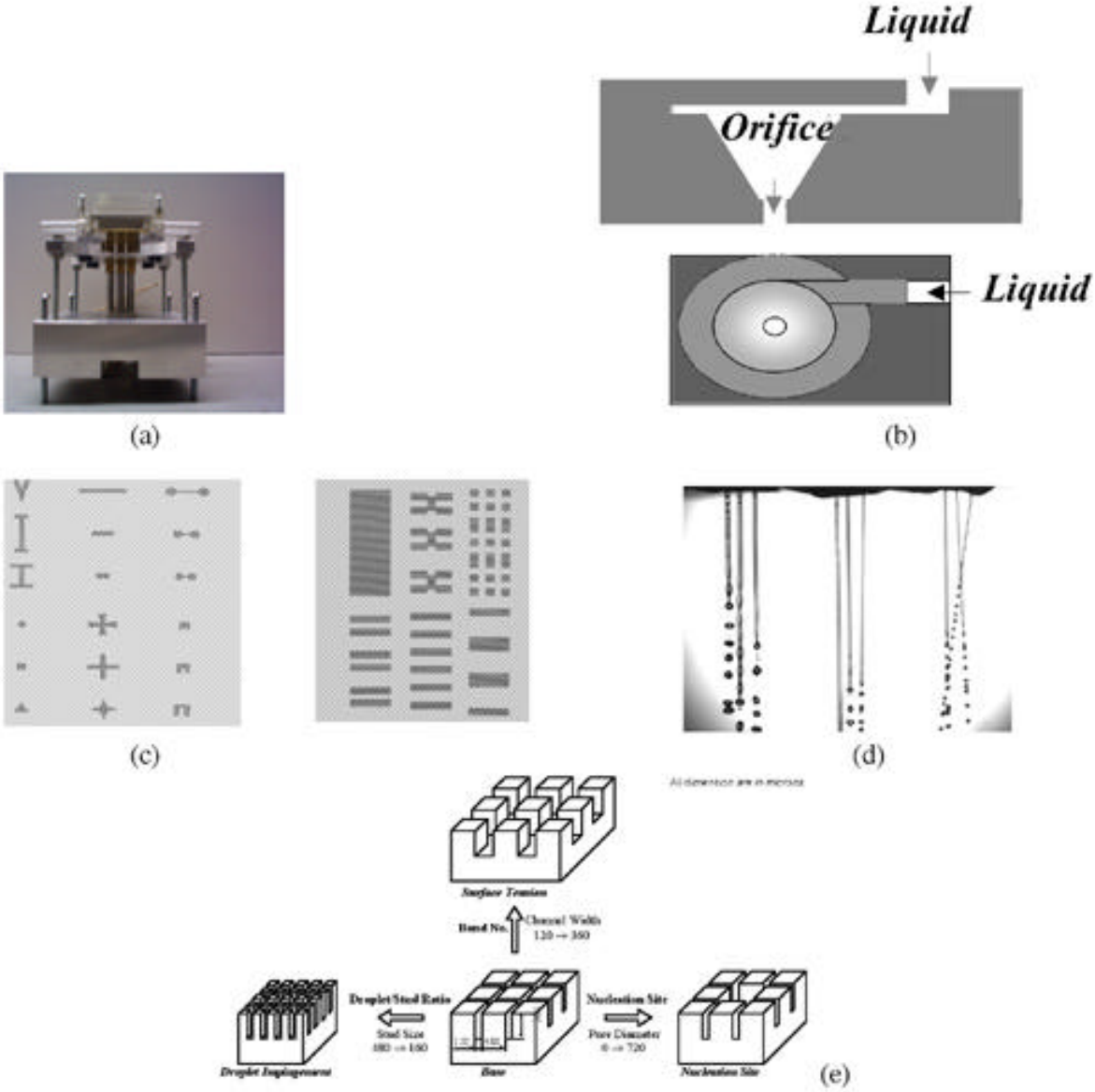


Figure 1: (a)Test Rig. (b) Micro-Nozzle Design, (c) Nozzle Orifice and Turbulence Promoter, (D) Micro-Jet Break-Up Lengths for Orifice shapes, and (e) Chip Surface Enhancements to Promote Nucleation.

Performer: Florida International University

Integrated Thermal Management using Laminate and Ceramic-MEMS Technologies

PI: Professor W. Kinzy Jones 305-348-2345

Other Team Members:

Mr. Mike Newton, Harris Coproration
Agent: ONR

Dr. Colin E. Wood 703-696-4218

Project Goals

The primary goal of this project is to develop an integrated approach to thermal mangement which can be integrated at the interconnect substrate level. The system uses a new heat spreader, which operates on a principle similar to heat pipes and an active fluid pumping system based on a piezo-driven micropump, both fabricated within the low temperature cofire ceramic interconnect substrate.

Approach

- Develop a heat spreader which will transfer heat from a concentrated high load source (200W/cm^2) to a large area for removal. Heat transfer within the substrate will approach effective thermal conductivities over 10,000W/mdegK.
- Fabricate a non-moving-part (NMP) micropump which is embedded in the substrate
- Integrate both into a complete thermal mangement system

Accomplished Milestones

- Initial heat spreader fabricated and sucessly tested at the level of 10 W power
- Test strcutures were fabricated that operated in the 80 W/cm^2 power region
- LTCC materials from 4 suppliers (7 tape types) were evaluated for materials properties (wetting performance, structural, mechanical, electrical) and manufacturability (thermal vias, lamination)
- Scaled NMP pump fabricated in plastic using SLA prototyping

Near-Term Milestones

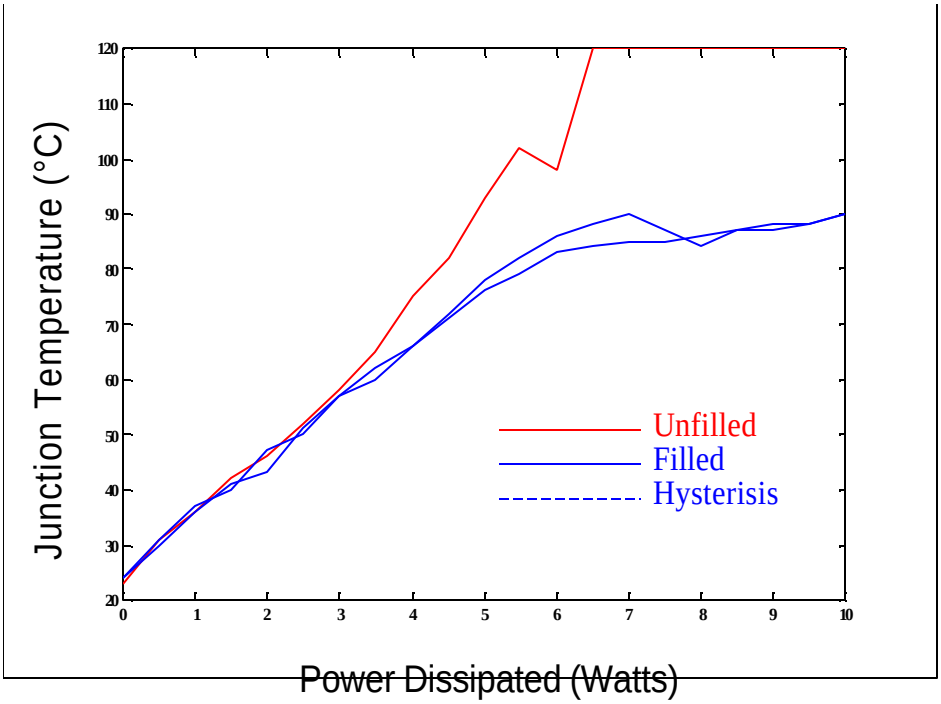
- Complete characterization and optimization of heat spreader
- Fabricate NMP pump with exterrnal piezo-driver in LTCC using both Tesla and convergent/divergent vales
- Fabricate micro heat exchanger to interconnect heat spreader with fluid pump system

Long-Term Milestones

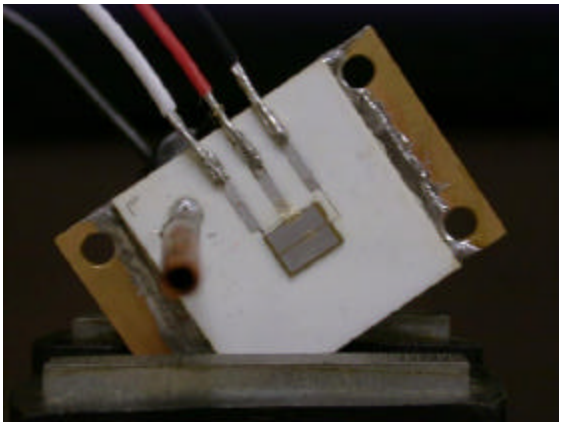
- Build integrated heat spreader with piezo-driven fluid pump liquid cooling
- Characterize performance to determine maximum power capacity of integrated design

Demonstration Activity

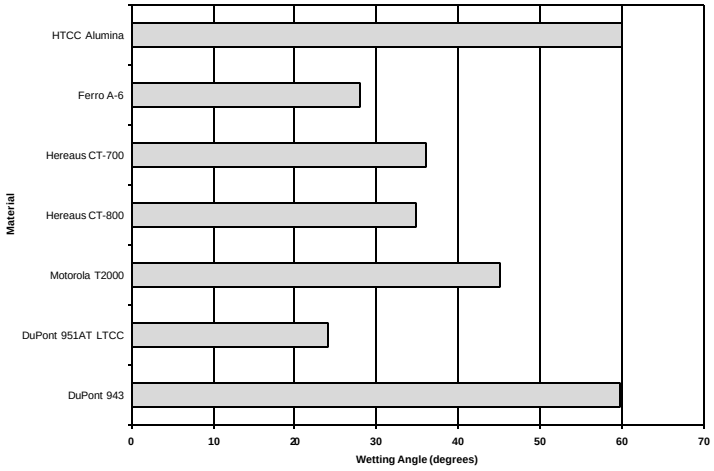
Heat spreader demonstrated. Near term, micropump and heat exchangers will be demonstrated. Long term demonstration is an interconnect substrate with each of the previously demponstrated components integrated into a function thermal management module.



- Initial Heat Spreader (filled with water as working fluid) Testing to 10 W



LTCC Heat Spreader



Wetting Angle as a function of LTCC Supplier

Performer: Georgia Institute of Technology

Microfluidic Technologies for Integrated Thermal Management: Micromachined Synthetic Jets and VIDA Heat Transfer Cells

PI: Professor Ari Glezer (404) 894-3266

Other Team Members:

Honeywell Technology Center, Dr. Eva Strzelecka
Intel Corporation, Mr. Benson Inkley and Dr. Murli Tirumalla

Agent: NSWC-Crane

Mr. J. W. Harms (812) 854-2398

Project Goals

The Georgia Tech HERETIC program focuses on the development and demonstration of microfluidic-based, thermal management technologies for electronic components having a diverse range of heat loads. Fluidic-based cooling approaches include phase-change heat transport based on vibration-induced droplet atomization (VIDA), and controllable heat convection using micromachined synthetic air jet arrays. These cooling technologies are demonstrated in two application areas: i) low-total-power, but high-power-density laser-diode arrays (with Honeywell) that are cooled using arrays of micromachined synthetic air jets, and ii) high-power dissipation in high-speed microprocessors (with Intel) using a compact, VIDA-based, phase-change heat transfer cell. Specific emphasis is placed on the integration with hardware using micromachining and electronic packaging techniques.

Approach

The Georgia Tech HERETIC program is comprised of the following elements:

(a) Characterization of the fluid mechanics and heat transfer properties of synthetic jet arrays for optimal substrate cooling and temperature distribution
(b) Development of a microjet-based active cooling substrate (ACS) that incorporates the fluidic functionality necessary to direct synthetic jets onto the electronic circuitry to be cooled
(c) Development of an active heat sink integrated with microjets to enhance the heat-sink effectiveness and its coupling to the global thermal-management system
(d) Development of a two-phase VIDA heat transfer cell
(e) Testing of the ACS for cooling of VCSEL arrays (with Honeywell), and the VIDA Cell for cooling of high-speed microprocessors (with Intel)

Accomplished Milestones

- The flow field of arrays of free and impinging synthetic jets has been investigated using particle image velocimetry (PIV) with specific attention to jet interactions and entrainment
- A prototype heat sink integrated with synthetic-jet actuators and an Intel Pentium test die was designed and tested
- A prototype VIDA-based heat transfer cell that is capable of removing 100W at 110^{o}C and internal pressure of 4.5 psia was designed, constructed, and tested
- A thermal test element for microjet-cooling assessment that enables simultaneous generation of heat and direct temperature measurement was microfabricated
- ACS for with integrated synthetic jets was developed for a 1-D VCSEL array
- Honeywell completed epitaxial growth of 670 nm VCSEL material and designed a mask set for 1-D arrays (100-element, 75 micron pitch and 150-element 50 micron pitch)
- A CFD model of the initial VIDA fin array design was developed

Near-Term Milestones

- Characterization of substrate cooling and by direct impingement of microjet arrays
- Linear arrays of integrated thermal test elements will be microfabricated and integrated into ACS designs to provide microjet-cooling assessment
- Laminated microjet driver diaphragms for ACS will be fabricated and tested
- Active microjet modulators will be developed
- Laminated ACS modules that include fluidic channels will be fabricated and tested
- Honeywell will fabricate, test, and characterize 670 nm 1-D VCSEL arrays
- The Honeywell 1-D VCSEL array will be integrated with ACS and thermally tested

- Active heat sink integrated with synthetic jet arrays and a central driver will be developed
- An evacuated VIDA-based heat transfer cell capable of a heat removal up to 100 W/sq cm at temperatures below 100^{o}C will be developed and tested with Intel's Pentium test dies
- CFD models for the ACS and the VIDA cell will be developed using CFDRC codes

Long-Term Milestones

- The flow field and the spatial and temporal heat-removal effectiveness of modulated microjet arrays will be characterized
- An active heat sink suitable for integration with a VIDA cell will be developed and tested
- Integrated drivers for VIDA will be developed and will be characterized based on the spray droplet size and velocity
- An ACS integrated with laminated jet drivers, fluidic passages, flow modulators, and electrical connections will be developed and tested
- Hybrid integration of VCSEL arrays with an ACS will be developed and tested to evaluate optical performance and manufacturability
- A controllable, low-pressure VIDA cell rated at power levels that exceed 120 W will be developed, integrated with Intel's next generation microprocessor, and tested
- Guidelines for the design optimization of both the ACS/VCSEL hybrid and the integrated VIDA cell will be provided using CFD models and associated experimental data

Demonstration Activity

The Georgia Tech HERETIC program includes two test vehicles that will be developed in collaboration with the industry partners. The first vehicle, an ACS (active cooling substrate) integrated with high-density 670 nm VCSEL arrays, is being developed with Honeywell Technology Center. Honeywell is currently designing a high-density linear 670 nm VCSEL array for this project, while the ACS is being developed at Georgia Tech. The second test vehicle is a VIDA heat transfer cell suitable for high-speed microprocessors (nominally 120 W, 100 W/cm^2). The first operational prototype of such a VIDA cell was recently completed and tested. The next version will be integrated with an Intel test die.

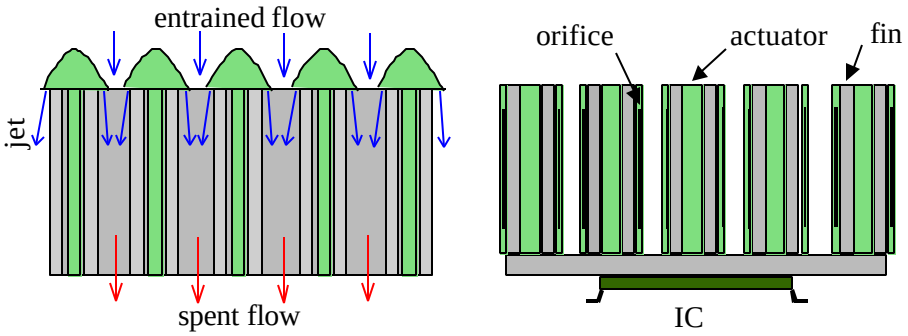


Figure 1 Heat sink integrated with synthetic jet modules: top view (left) and side view (right). The heat sink tested (8.1 x 4 x 3.5 cm) dissipates 49.9W using a thermal test die at 70°C.

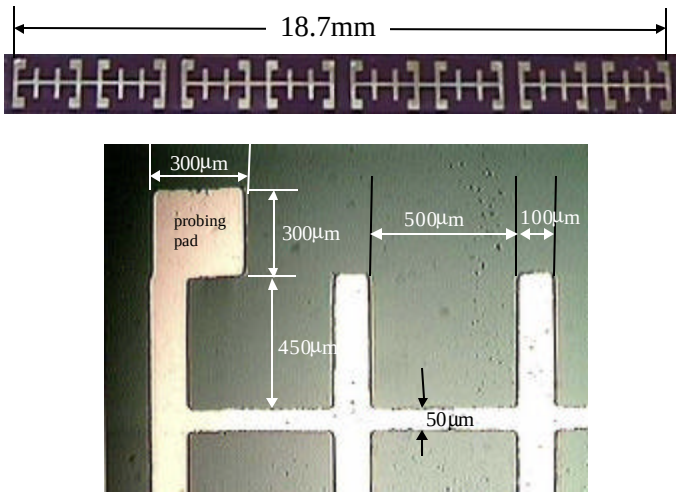


Figure 2 A microfabricated four-segment linear array of integrated platinum thermal test elements for microjet cooling assessment (top). The array enables simultaneous generation of heat and direct measurement of element temperature. Each element within a segment is 500µm long and 50µm wide (bottom).

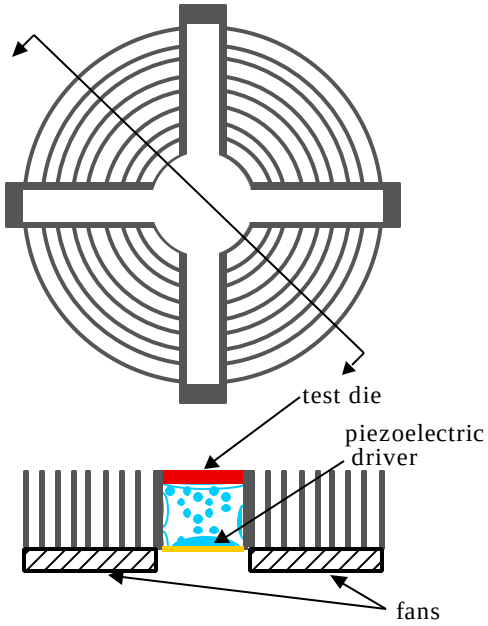


Figure 3 Prototype of VIDA heat transfer cell (OD ≈ 10 cm). The cell removes 100W at 110°C and 4.5 psia.

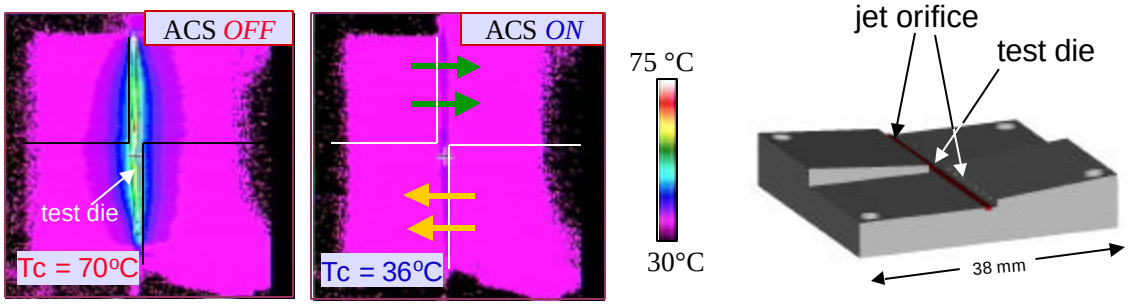


Figure 4 ACS module with two integrated synthetic jets and a linear test die (right), and top-view infrared thermal images of the ACS with and without active jets.

Performer: Jet Propulsion Laboratory/California Institute of California

Monolithically Integrated Thermoelectric Coolers for Mid-IR Lasers

PI: Dr. Jean-Pierre Fleurial (818) 357-4224

Other Team Members:

Boston University, Professors Selim Ünlü and Bennett Goldberg
UCLA, Professor Gang Chen
University of Houston, Professor Shin Shem Steven Pei

Agent: AFOSR/NE

Major Daniel K. Johnstone (703) 696-7545

Project Goals

This program seeks to address areas of interest to the HERETIC program: thermal management device development, integration and packaging, modeling and simulation and a focused system demonstration. The main objective is to integrate novel solid state thermoelectric microdevices with mid-IR lasers to achieve transient deep spot cooling of the laser active region. Successful development of monolithically integrated thermoelectric microcoolers (TEMC) with mid-IR lasers operating under pulsed conditions will free such lasers from the requirement of liquid cryogens and provide compact, low cost IR, and coherent IR sources for both military and commercial applications. The project team has expertise in thermoelectric materials and devices, mid-IR lasers and microfabrication, as well as thermal design, modeling, high resolution imaging and testing. Key results expected from this program are: software packages for the design of TEMC and for the thermal modeling of mid-IR lasers, novel TEMC configurations with enhanced performance under transient operation, high-resolution thermal imaging instrumentation tools based on solid immersion lens and time-resolved Raman microscopy, and integrated TEMC/mid-IR laser packages demonstrating improved laser power output.

Approach

This project is focusing on the development of some key technologies:

- Advanced thermal modeling tools for the thermoelectric microdevice, mid-IR laser and their interface, including a physical understanding of relevant thermionic and thermoelectric processes
- Design, fabrication and testing of highly miniaturized monolithically integrated thermoelectric microcoolers operating under transient conditions
- Ultra-high resolution thermal imaging microscopy to meet the need for thermal characterization and modeling of the mid-IR laser devices and interfaces to be cooled, as well as future industry needs
- Direct integration of mid-IR lasers with near room temperature solid-state packaging and demonstration of significantly enhanced performance

Accomplished Milestones

Thermoelectric microdevice processing steps allowing for prototype fabrication have been developed. Miniature bulk devices ready to be tested under pulsed current.

- Thermal conductivity of InAs/AlSb superlattice structures measured as a function of growth temperature and post-growth annealing.
- Conducted initial model calculations for designing thermoelectric microdevice and predicting performance under high current pulsed operation.
- Potential for sub-micron resolution using a silicon Solid Immersion Lens (SIL) demonstrated.
- Micro-Raman temperature-dependent data on laser substrate material (GaSb) obtained.

Near-Term Milestones

- Test the performance under transient/pulsed operation condition of advanced miniature bulk thermoelectric coolers
- Develop detailed models for the steady-state and transient response of the thermoelectric microcoolers (TEMC)
- Initiate fabrication of TEMCs using a combination of electrochemical and integrated circuit techniques
- Develop thermal models for the IR lasers that include the side effects on the thermal conductivity of the superlattice structures used for the mid-IR lasers
- Explore new physics to further enhance cooling effects in the laser and TEMC structures/devices. Both thermoelectric and thermionic effects will be considered.
- Complete fabrication of a solid immersion lens (SIL) mid-infrared microscope and measure laser superlattice and thermoelectric microdevice structures
- Study issues associated with the fabrication of integrated packages and testing of the laser and TEMC performance

Long-Term Milestones

- Prototype of novel thermoelectric microcooler (TEMC)
- Integrated mid-IR laser/thermoelectric microcoolers packages. The thermal management effectiveness will be demonstrated by significantly increased laser output power under pulse operation mode compared to similar lasers running at the same heat sink temperature.
- High-resolution thermal imaging instrumentation based on Solid Immersion Lens microscopy
- Time-resolved Raman microprobe optimized for the thermal imaging of mid-IR lasers
- Software packages for the design of thermoelectric microcoolers, and for the thermal modeling of mid-IR lasers
- Results of application of new thermal modeling and imaging tools to other selected optoelectronic devices and components for evaluating potential thermal management solutions based on proposed concepts

Demonstration Activity

We will use thermal modeling, imaging and novel solid state thermoelectric microcoolers to demonstrate that monolithically integrated mid-IR laser/microcooler packages will allow for near-room temperature operation of these lasers with a significant increase in the power output compared to similar lasers operated at the same heat sink temperature

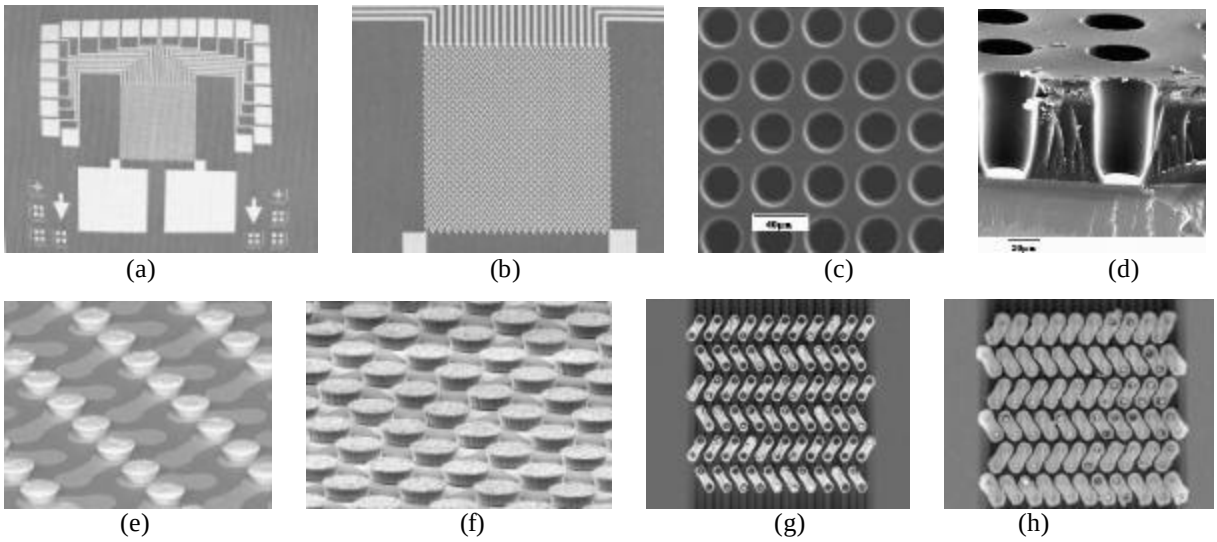


Figure 1: Thermoelectric Microdevice Fabrication; (a) Photolithographic mask; (b) Patterned bottom interconnects (sputtered); (c) and (d) Thick photoresist template; (e) electrodeposited n-type Bi_2Te_3 legs onto bottom interconnects; (f) Two sets of legs electrodeposited; (g) Thin film metal top interconnects (sputtered) patterned on top of microlegs and (h) electrodeposited thick metallic interconnects to complete self-standing device

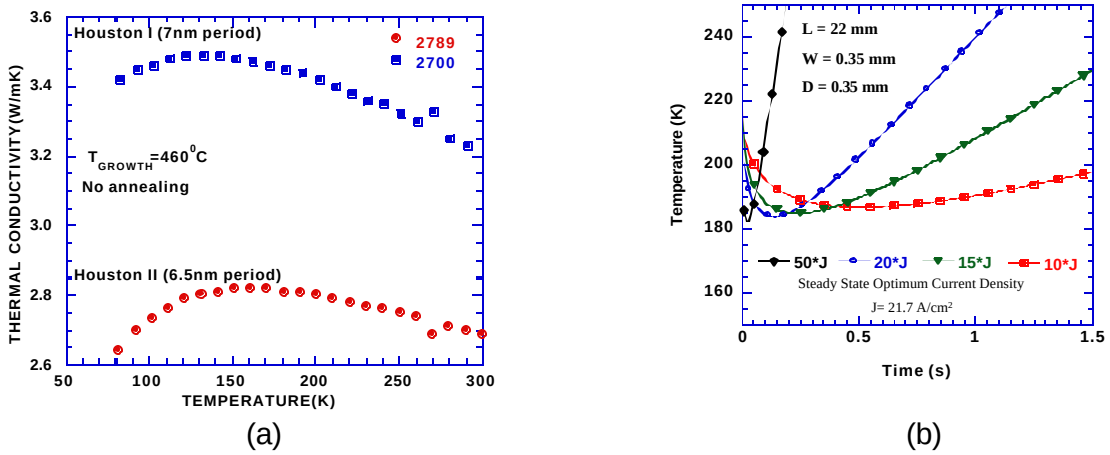


Figure 2: Experimental and theoretical thermal analysis; (a) Thermal conductivity as a function of temperature for mid-IR laser superlattice structures with different periodicity; (b) Predicted 40K enhanced cooling effect for high aspect ratio (tall, thin legs) bulk thermoelectric device when pulsed with different current intensities in addition to the steady-state operation.

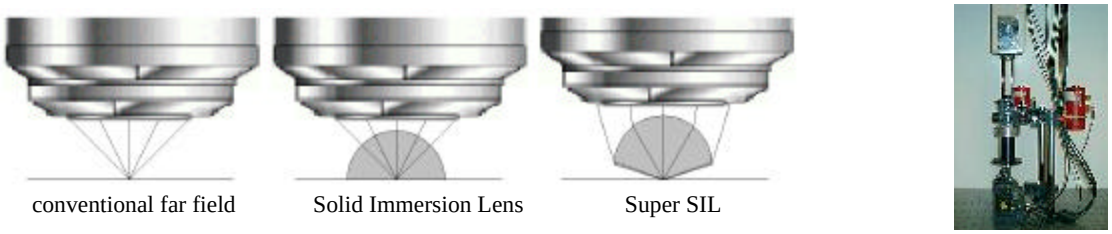


Figure 3: Schematic representation of the approach to ultra-high resolution thermal imaging using a solid immersion lens (SIL) and experimental setup for two-color imaging.

Performer: Rockwell Science Center

Chip-Level Thermal Management Using MEM Thermoacoustic Refrigerators

PI: Jeffrey DeNatale (805) 373-4439

Other Team Members:

Rockwell Science Center, Drs. Chung-Lung Chen and J. Jason Yao
Johns Hopkins University, Dr.-Ing. Cila Herman
University of Missouri, Professor Hongbin Ma

Agent: AFRL/IFSC

Mr. Stephen Benning (937) 255-4709 x4170

Project Goals

The goal of the Rockwell-led HERETIC project is the development and demonstration of a miniaturized refrigeration device based on the thermoacoustic refrigeration principle. This technique utilizes high-frequency acoustic energy to provide the heat pumping effect. To achieve this goal, program efforts are focused on the development and integration of key component technologies:

- Theoretical modeling of the thermoacoustic effect at small spatial dimensions
- Piezoelectric materials and transducers for high-efficiency acoustic generation
- Micromachined thermoacoustic stack components for device miniaturization

Approach

Development and integration of key component technologies:

- Theoretical modeling of thermoacoustic effect at reduced size scale
- Micromachined thermoacoustic stack structures
- High-performance piezoelectric acoustic transducers

Accomplished Milestones

- Numerical predictive codes for macro-TAR design have been exercised to provide initial design guidelines
- Piezoelectric materials have been selected for initial acoustic actuator development. Actuator structures for displacement amplification have been evaluated, and preferred designs selected.
- Micromachined TAR stack designs and process tolerances have been evaluated using test structures, and selected designs scaled up to larger-area processing
- A prototype TAR testbed has been developed using COTS components to support component evaluation and testing

Near-Term Milestones

- Integrate micromachined Si TAR stack elements into prototype testbed to evaluate impacts of design parameters on thermal performance
- Refine acoustic transducer elements for increased resonance frequency and amplitude
- Begin experimental development of alternate stack materials and structures
- Integrate heat exchangers into prototype testbed

Long-Term Milestones

- Develop compact, high-performance acoustic drive components
- Develop micromachined TAR stack structures and materials for high-efficiency operation
- Develop compact heat exchangers to support integration with electronic chips
- Integrate component technologies into compact packaged MEM-TAR module and demonstrate refrigeration performance

Demonstration Activity

We will develop a proof-of-concept demonstration of a miniaturized TAR device (MEM-TAR), and demonstrate its utility for chip-level thermal management through integration with an electronic device

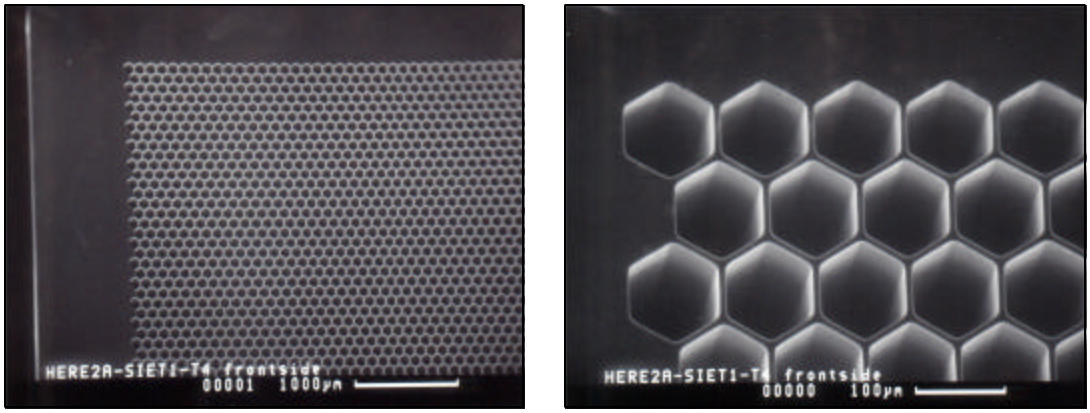


Fig. 1: SEM micrographs of micromachined Si stack structure

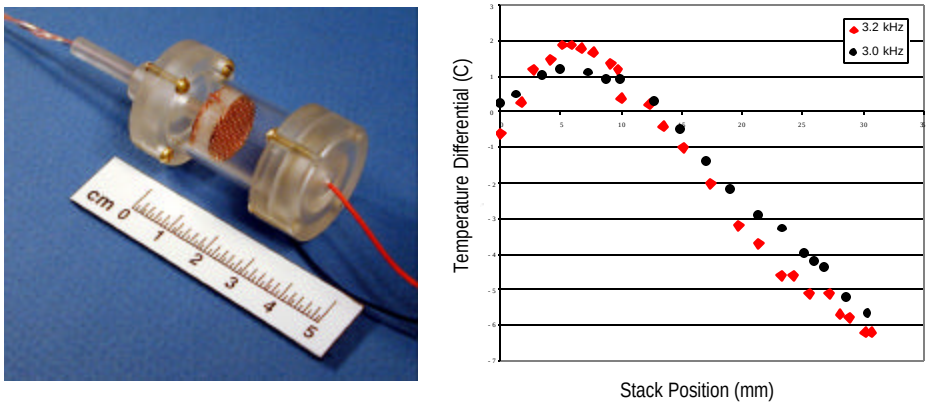


Fig. 2: Prototype TAR assembled from COTS components (left); Temperature difference across stack as a function of stack location for initial prototype TAR (right)

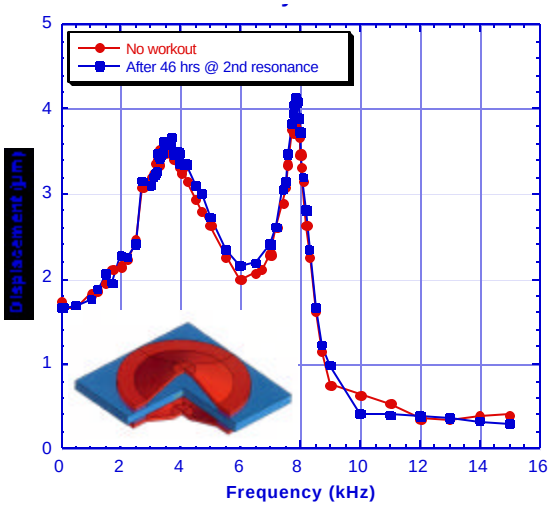


Fig. 3: Low-amplitude frequency response of piezoelectric actuator

Performer: Stanford University

Electrokinetic Micro Coolers

PI: Professor Kenneth Goodson (650) 631-7542

Other Team Members:

Stanford University, Professors Juan Santiago and Tom Kenny
Intel Corporation, Drs. Harry Fujimoto and John Carruthers

Agent: AFRL/IFSC

Mr. Stephen Benning (937) 255-4709 ext 4170

Project Goals

This project develops two-phase cooling systems removing 200 W from 2 cm x 2 cm IC chips using electrokinetic pumps for the liquid phase and micromachined evaporators. Supporting goals include the development of high-flowrate electrokinetic pump technology, the characterization of two-phase flow regimes in microchannels, and the development of micromachining technology for pumps and heat exchangers and manufacturing processes for integrating the coolers with Intel chips. An additional, higher-risk goal is to develop refrigeration devices based on novel compressors for the gas phase using electrokinetic technology.

Approach

The project will fully characterize and optimize system sub-components, and integrate them into a stable cooling loop that is compatible with Intel IC and packaging technology. Sub-components:

- Electrokinetic liquid pump with flowrate ~10 ml/min and pressure ~2 atm
- Micromachined evaporator (microchannels)
- Large-area condensor

Accomplished Milestones

- High-flowrate EK liquid pump in a free-standing capillary (6 ml/min)
- Design and micromachining of microchannel evaporators, with integrated temperature sensors, from silicon and glass
- Micron-scale PIV imaging of turbulence transition in microchannel evaporators
- Temperature-flowrate measurements in two-phase microchannel evaporators, including a preliminary study of the critical heat flux

Near-Term Milestones

- A single-phase EK convector device (year-1 demo). This requires combination of pump and microchannel technology into a closed-loop system, which removes approximately 25 W from a silicon heater/thermometer chip.
- Characterization and optimization of pressure/flowrate regimes in two-phase EK-pumped microchannels. This is achieved using micromachined two-phase flow systems with integrated temperature sensors, together with microscope bubble visualization and particle imaging velocimetry (PIV).
- Development of integrated microchannel/pumping technology in a single substrate.

Long-Term Milestones

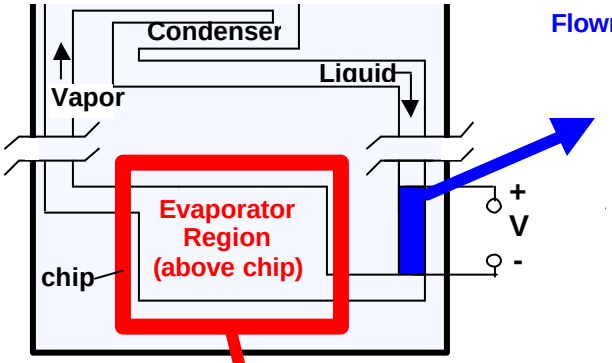
- Design and fabrication of novel convectors in silicon. This will use anisotropic etching technology to yield higher convection rates than are available with conventional microchannels. Examples include liquid nozzle jets.
- Detailed modeling and evaluation of candidate refrigeration cycles using EK pumps.
- A two-phase integrated EK convector (year-2 demo). This demonstrator will remove 100 W from silicon demo heater/thermometer chip and show the feasibility of a two-phase loop.
- Detailed optimization of pressure-flowrate regimes in two-phase EK-pumped micro jets and micro channels. This will build upon the preliminary modeling performed for 1Q00, but will involve more experimental data from the year-2 demonstrator. We anticipate much effort on the optimization of the quality of the exiting fluid.

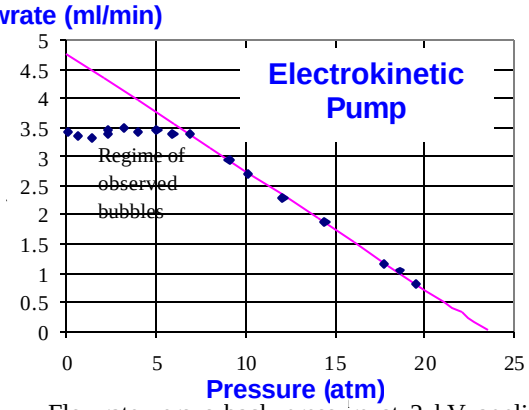
Demonstration Activity

Demonstration of an optimized two-phase EK convector prototype. The device will attach to the backside a test chip from Intel and remove 200 W.

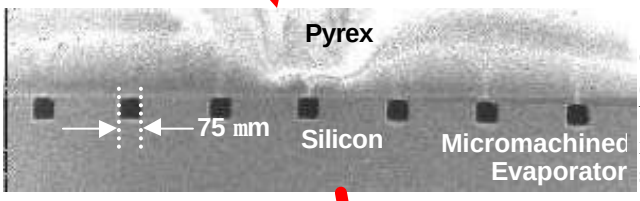
Demonstration at Stanford of an integrated refrigeration demonstrator device, micromachined onto a single plate.

Electrokinetic Micro Cooler

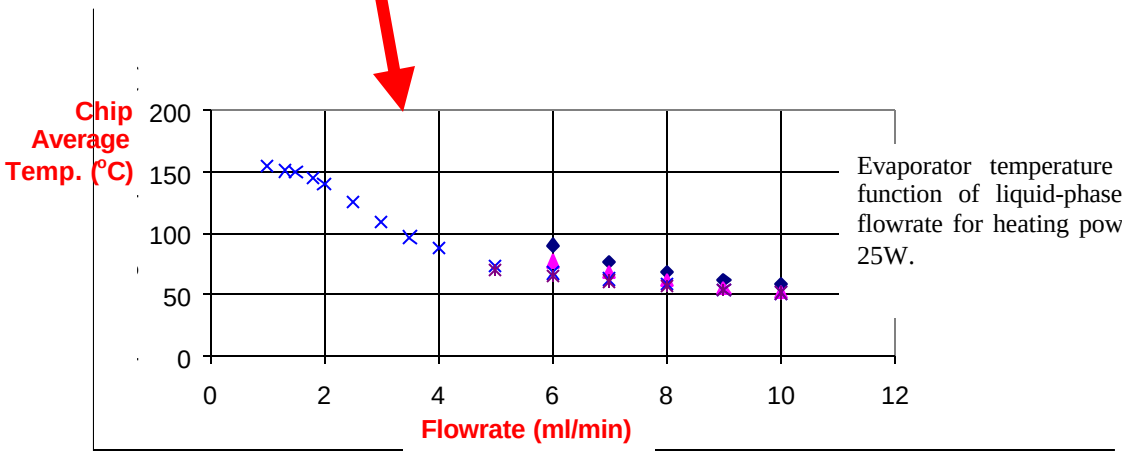




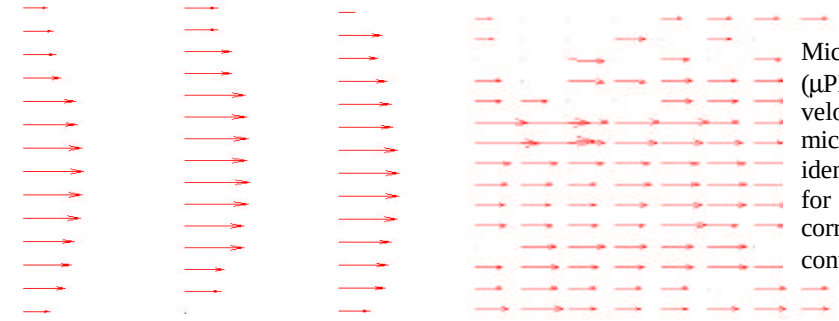
Flowrate versus back pressure at 2 kV applied voltage for an EK pump developed under HERETIC.



Cross-sectional scanning electron microscopy (SEM) image of evaporator region, showing the bond between pyrex and silicon. The evaporator includes integrated doped-silicon temperature sensors (not shown) for characterization.



Evaporator temperature as a function of liquid-phase inlet flowrate for heating power of 25W.



Microscale particle image velocimetry (μPIV) data for liquid water flow velocity profiles in evaporator microchannels. These measurements identify the critical Reynolds number for the onset of turbulence and a corresponding improvement in convection.

Performer: University of California, Berkeley

Integrated Micro-Cooler Module for High Thermal Flux Removal

PI: Professor R. Greif (510) 642-6462

Other Team Members:

UCB, Professors C. Grigoropoulos, D. Liepmann
Air Force Research Laboratory, Wright-Patterson Site, Dr. K. Yerkes
Harris Corporation, Mr. M. Newton, Mr. Tebbe, Ms. C. Gamlen

Agent: Space and Naval Warfare Systems Center

Dr. Dr. Cynthia Hanson (619) 553-5242

Dr. Stephen D. Russell (619) 553-5502

Project Goals

The goal of the project is to develop an innovative and robust micro-cooler module to provide integrated cooling and thermal management to electronic components and to systems. This will reduce operating costs and improve system performance including reliability. The micro-cooler module embodies a multi-port micro capillary pumped loop (CPL) which has broad capabilities and applicability including cooling at the chip level and heat removal to regions away from heat sources. Advantages include precise temperature control at the chip level with efficient cooling because specific heat sources are targeted; this results in a small overall size of the integrated electronics system and cooling package. To demonstrate specific capabilities a 75 amp, 600 volt Insulated Gate Bipolar Transistor (IGBT) Intersil has been targeted. This device is used for aircraft motor control operations as well as for other high power voltage switching applications.

Approach

The evaporator of the micro-CPL is fabricated directly within the wafer to provide efficient cooling. Determination of the heat transport and flow, including evaporation and condensation, in a multi-port micro-CPL platform establishes the cooling potential of the device. Integration of the micro-CPL with an IGBT and operation of the system provides the capability of an integrated module.

Accomplished Milestones

- Micro-CPL platform designed and fabricated.
- Test facilities at AFRL and UCB have been constructed. Experimental apparatus specific to the testing of prototype and next generation micro-CPLs is being assembled at AFRL.
- Testing conducted at AFRL and at UCB. Device demonstrated to work as a micro-CPL. Reservoir locations have been determined. Posts for liquid isolation in the evaporator are found to be unnecessary. New designs for micro-CPL completed and fabricated.
- Completed package design by Harris Corp. for incorporation of micro-CPL with an IGBT.
- Analytical tools to aid in micro-CPL design and operation.

Near-Term Milestones

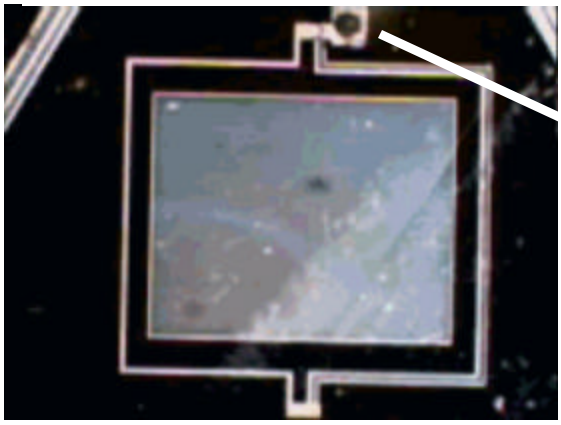
- Testing of new micro-CPL devices. Measurements of start-up, evaporation and condensation under varied conditions.
- Harris Corp. testing and evaluation of the micro-CPL cooling capability, by a single-component (IGBT) thermally enhanced BGA package. Data to be compared to test vehicles which utilize traditional thermal management practices.
- Analytical tools to aid in experimental evaluation, thermal device isolation capability and system design.

Long-Term Milestones

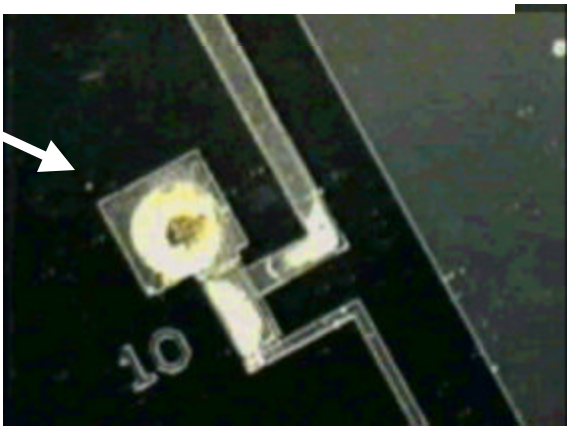
- Complete component and system testing. Operational capability and energy transport potential.
- Measurements of micro-scale heat transfer and fluid dynamics.
- Multicomponent thermal management with efficient heat dissipation.
- Analysis of micro-scale transport, transport potential and system operation.

Demonstration Activity

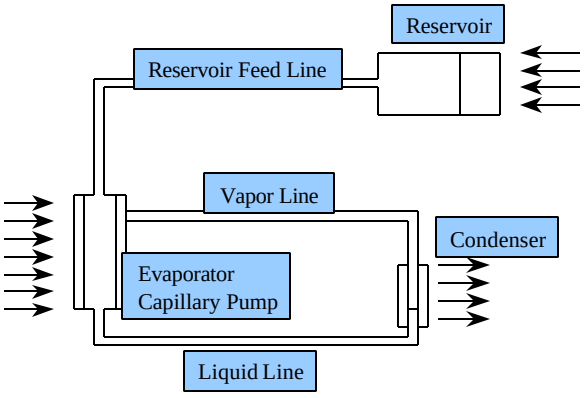
Full system demonstration of thermal management of multi-component fiber optic transmitter module with an integrated micro-CPL module.



Initial micro-CPL prototype fabricated of Si with glass cover and external reservoir

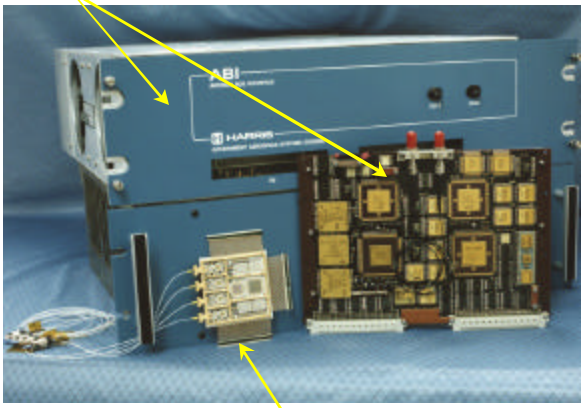


Operational micro-CPL showing steady state evaporator operation



Schematic of the microCapillary Pumped Loop shown above.

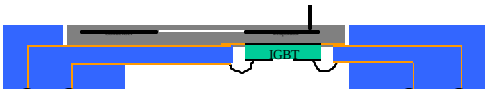
2 Channels - Chassis and SMT Examples

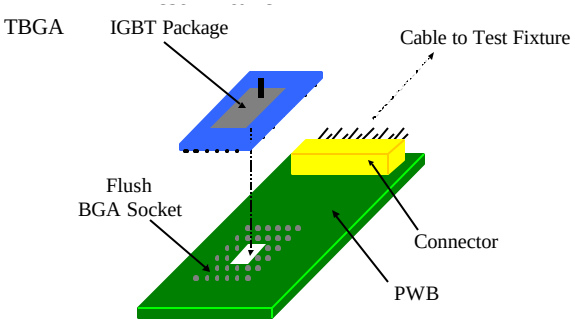


4 Channel MCM

Demonstration of the increased functionality and decreased size of a high-speed data bus for the F-22 aircraft by the use of multi-Chip Modules (MCM). Cooling becomes a critical factor in further size reductions.

TBGA IGBT Package





IGBT Test structure. This system is currently being constructed and will be used to test the micro-Capillary Pumped Loop using an IGBT as a temperature source. This system will allow precise control of energy input to the microcooler system

Performer: University of California, Los Angeles

Modular Micromachined SI Heat Removal (MOMS-Heat Removal)

PI: Professor Ivan Catton (310) 825-5320

Team Member Organization:

UCLA, Professors Elliott Brown, Vijay K. Dhir and C.J. Kim
Thermacore Corporation, Dr. Mark North
Rockwell Science Center, Dr. Mike Shaw

Agent: ARO

Dwight Wollard (919) 549-4297

Project Goals

The primary goal of the project is to develop two core technologies for cooling power- electronic devices (integrated MEMS microjet arrays, and integrated biporous heatpipes) and to demonstrate their capabilities by full system testing of: (1) a 30-W RF or higher power MOSFET for wireless transmitters, and (2) an IGBT of the 15-hp-class or higher solid-state motor drives.

Approach

Develop "chip to air" integrated cooling systems based on the two core technologies, demonstrate feasibility of the concepts with laboratory experiments both at the component as well as the module level, and then design and construct complete thermal management systems for full system tests. The "chip to air" cooling system is composed of one of the core technologies and an augmented surface for the interface between the system and air.

Accomplished Milestones

- Heat fluxes as high as 220 w/cm^2 have been obtained with air water sprays at surface temperatures less than 105°C. A loop for testing the water spray condenser and final heat rejection to the ambient has been developed.
- An Evaporation-Boiling-Evaporation (EBE) model for thick biporous wicks and an evaporation model for thin biporous media were developed that describe heat transfer in biporous wicks. Heat pipes for IGBT cooling have been designed and the evacuating and filling facility of heat pipes has been assembled.
- Fabrication of the first round of microinjectors has been completed. Based on the testing results, mass flow rate and power consumption estimated. Projected power consumption appears excessive.
- The design of candidate heat sink surfaces has been completed. A method of optimization of simplified regular interfacial shapes based on statistical design of experiments (DOE) approach has been developed with supporting heterogeneous flow and heat transport models and an approach for closure of the heterogeneous terms in the governing equations. The experimental test facility to support this task has been completed.
- Working with the Rockwell Science Center and Thermacore, the UCLA team has designed and begun fabrication of a model IGBT/diode package. The design includes an integral planar heatpipe for demonstration and experimental analysis as a single-phase (half-bridge) of a standard three-phase solid-state motor drive. The IGBTs and diodes are commercial parts (IXYS Corporation).

Near-Term Milestones

- Develop a pulsing droplet concept and experimentally determine the heat fluxes that can be achieved. Develop a condenser design and test it for ultimate heat rejection to the ambient.
- Develop a final heat pipe design for IGBTs and begin design of a heat pipe module for MOSFET cooling. Develop a thermal/electrical model of the MOSFET to allow optimization of a special biporous media with grooves and maximize the heat transfer crises in biporous media.
- Develop an alternative approach to the present thermal droplet injection being studied. The present candidate is piezo disk pumping.
- Complete implementation of the DOE method of optimization of heat rejection: develop methods for numerical evaluation, data reduction and analysis of design results, and provide first preliminary DOE calculations based on two level point parameters for laminar and turbulent regimes.
- Begin heat transfer experiments to calculate the thermal resistance of several candidate heat sinks, use Laser Doppler Velocimetry to experimentally analyze the flowfield around the candidate heat sinks and a numerical code to predict performance of candidate heat sinks.
- Complete the packaging (soldering, wirebonding and insulation) of the silicon IGBTs and diodes with the Thermacore heatpipes on commercially supplied direct-bond copper/alumina substrates (Curamik-Thermalloy) and carry out

experimental electrical and thermal investigations of the packages with the half-bridges driving resistive and inductive loads. Analyze experimental data to determine the improvement in electrical performance (power handling) of the IGBT half-bridge as a function of Tj up to approximately 200°C.

- Develop new package designs for integration of MOMS technology with power RF LD-MOSFETs. Heatpipes and microjets are being considered for this integration, although microjet arrays may be favored because of ease of integration on the top side of the MOSFET die.

Long-Term Milestones

- Develop a pulsed droplet concept and experimentally determine the heat fluxes that can be achieved with this concept. Develop a condenser design to support the pulsing drop conceptand test it for ultimate heat rejection to the ambient. Integrate the evaporator and condenser including the pump to develop a phase change cooling module that can accommodate high heat fluxes and prepare it for test with either an LD-MOSFET or IGBT.
- Optimize designs of the passive heat pipe modules for IGBT and MOSFET cooling and experimentally determine their performance. Prepare a complete system for IGBTs and MOSFETs to be delivered to Rockwell for packaging and testing.
- Develop a microsystem that wets heated silicon surfaces with streams of coolant.
- Develop an improved augmented surface for heat rejection to air that can be combined with either the pulsed droplet concept or the heat pipes to be used for IGBTs and LD-MOSFET. Experimentally confirm the models devloped and implementation of the DOE procedure.
- Package and test 30-W RF power amplifier using LD-MOSFETs (Polyfet, Inc.). The key goal here will be to get more RF performance at a given junction temperature than present packaging presently allows.

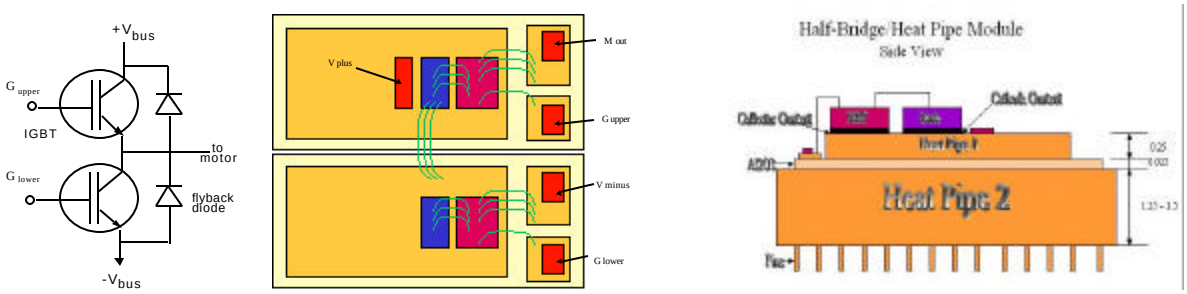
Demonstration Activity

Package and test 6-pack IGBT/diode inverter modules (with integrated MOMS heat removal devices) in a real solid-state 15-hp motor drive.

Package and test an LD-MOSFET in a real solid-state power electronics configuration.

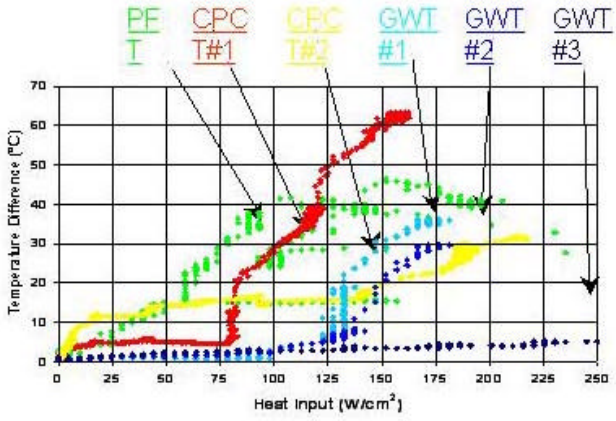
University of California, Los Angeles

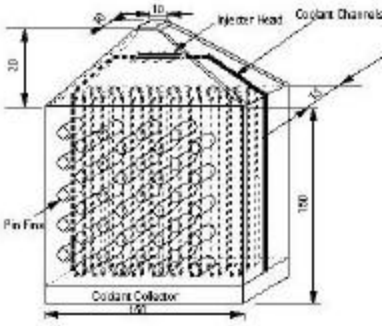
Working with the Rockwell Science Center and Thermacore, the UCLA team has designed and begun fabrication of a model IGBT/diode package. The design includes an integral planar heatpipe for demonstration and experimental analysis as a single-phase (half-bridge) of a standard three-phase solid-state motor drive. The IGBTs and diodes are commercial parts (IXYS Corporation). The schematic is shown below.



Schematic of the UCLA/Rockwell/Thermacore integrated planar heatpipe half-bridge design.

Tests of heat pipe wicking demonstrate the benefits of optimizing the biporous wicking. Note that type GWT #3 achieves a 250 w/cm^2 heat flux with only a 6 ^{0}C temperature drop (a very low thermal resistance). The surface temperature can be Pulsed water droplet injection schematic shown below has achieved more than 200 w/cm^2 with a heated surface slightly in excess of 100 ^{0}C.





Microjet Injector Utilizing Natural Convection for Heat Rejection to Ambient (All dimensions in mm)

Performer: University of California, Santa Barbara

Integrated Microelectronics and Photonics Active Cooling Technology (IMPACT)

PI: Professor John Bowers (805) 893-8447

Other Team Members:

University of California Santa Cruz, Ali Shakouri
University of California Berkeley, Arunava Majumdar
Harvard University, Venkatesh Narayanamurti
HRL Laboratories, Edward T. Croke III

Agent: ARO

Dwight Woolard (919) 549-4297

Project Goals

The primary goal of the IMPACT effort is to demonstrate the advantages of heterostructure integrated thermionic (HIT) coolers and their integration with microelectronics and photonics. The majority of our research involves the development of this new technology through nanostructured materials design and growth; device design and fabrication; simulation and modeling; novel measurements of thermoelectric and thermionic behavior; and systems integration and packaging.

Approach

Materials design is focused on increasing the cooling power and efficiency with thermionics and phonon bandgap engineering in superlattices. Electrical and thermal transport measurements are used to verify model predictions and aid in further improvements in device and materials design. Simulations are used to determine device limitations and non-ideal effects. Ultimately, thermionic devices are to be integrated and packaged for systems demonstration.

Accomplished Milestones

- InGaAs/InGaAsP superlattice thin film coolers have been integrated with InP p-i-n diodes. Net cooling has been measured with an additional heat generation density in the diode up to 90 W/cm^2.
- Integrated cooling by as much as 2.4 degrees at room temperature and 7.3 degrees at 150°C substrate temperature has been demonstrated with p-type SiGe/Si superlattice samples. This cooling over 3 micron thick barriers corresponds to cooling power densities approaching 1 kW/cm^2.
- Advances in material growth: SiGeC/Si superlattices lattice matched to Si, very thick $Si_{0.7}Ge_{0.3}$/Si superlattices up to 6 µm, and high Ge-content $Si_{0.4}Ge_{0.6}$/Si superlattices
- 3-ω measurements of thermal conductivity (77-400K) of various superlattice structures

Near-Term Milestones

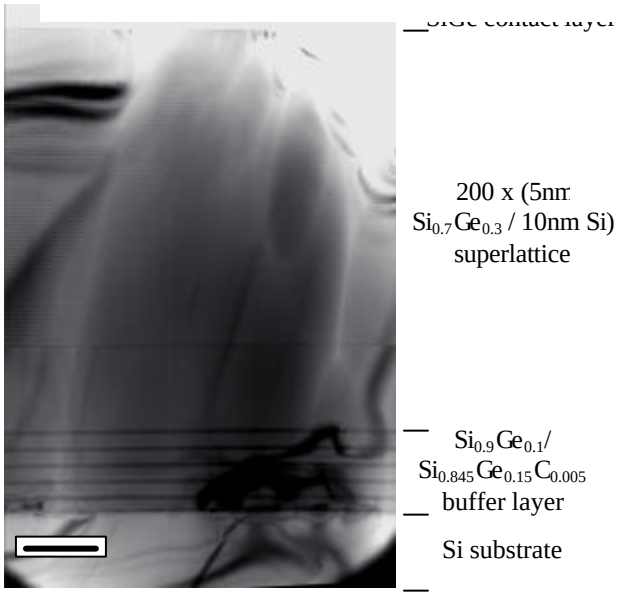
- Further development of n- and p-type superlattice cooler designs for future integration of p- and n-type elements
- Substrate transfer of thin films to copper or diamond substrates for improved heat sink properties
- Monolithic integration of InGaAsP/InP based thin film coolers with in-plane laser structures emitting at 1.55 µm
- Cross sectional thermal microscopy of thin film thermionic coolers with 20-40 nm resolution

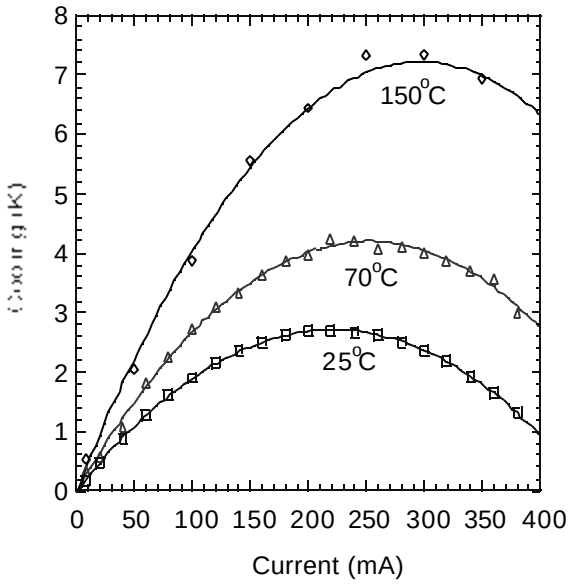
Long-Term Milestones

- Fabrication and characterization of multi element n- and p-type HIT coolers on InP and Si
- Integration of n- and p-type devices in the same package or on the same substrate to eliminate the extra heat load at the cold junction of the device
- Integration of HIT coolers with optoelectronic devices (VCSEL's), and VLSI chips
- Thermoelectromechanical cooler fabrication using surface micromachining techniques

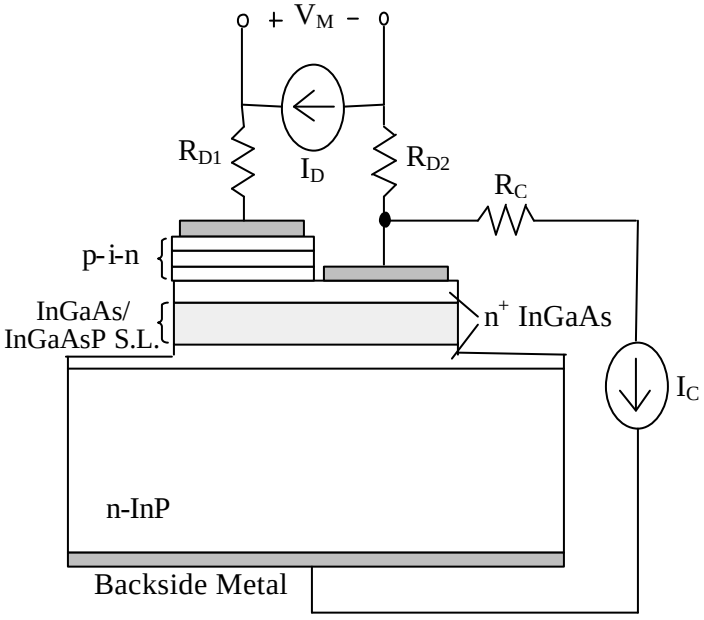
Demonstration Activity

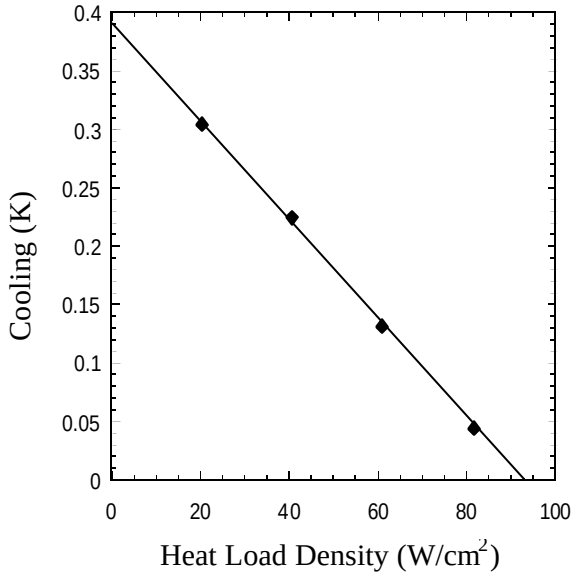
An integrated cooling array will be demonstrated with InGaAsP based HIT coolers on a 2" InP substrate and SiGe based HIT coolers on a 5" Si substrate. SiGe HIT coolers will be integrated with Si readout circuits to demonstrate spot cooling of selective devices on a VLSI chip. Finally, an array of VCSEL's will be integrated with an array of coolers to demonstrate individual cooling control over each VCSEL element.





The picture on the left is a TEM image of a MBE grown SiGe/Si p-type HIT cooler structure. The plot on the right shows the measured cooling for this structure on a 50 x 50 μm^2 size cooler at various substrate (heat sink) temperatures.





The diagram on the left shows the device structure for an integrated InP p-i-n diode and InGaAsP/InP HIT cooler. The temperature is determined from the temperature-dependent current-voltage characteristic of the diode, and the heat load on the cooler is varied by changing the current through the diode. The plot on the right side shows the measured cooling versus the excess heat load.

Performer: Massachusetts Institute of Technology

Research on Family of IV-VI-based Multi-layered Thermoelectric Material

PI: Professor Mildred S. Dresselhaus (617) 253-6864

Agent: Space and Naval Warfare Systems Center

Dr. Cynthia Hanson (619) 553-5242

Project Goals

The specific goals of the study are: (1) To confirm experimentally the prediction that the three-dimensional thermoelectric figure of merit *ZT* can be increased in Low Dimensional Structures by carrying out systematic studies on a family of related IV-VI based compounds, the first family of compounds to be studied systematically; (2) To reveal the main factors that influence the increase of *ZT* in a family of related superlattices (SLs); (3) To establish the conditions under which the *ZT* in SLs has a maximum value; and (4) To give a theoretical interpretation and experimental corroboration of the influence of various factors on increasing the *ZT* value in SLs.

Approach

Use various examples of the IV-VI family of superlattices to identify the general principles for increasing *ZT* through comparisons between model calculations and experimental measurements of the transport properties.

Accomplished Milestones

- A framework for IV-VI Based Superlattices has been laid out
- Superlattices of PbS/EuS have been fabricated, for several quantum well thicknesses, and preliminary measurements of the power factor have been made
- Progress has been made in developing a theoretical model for the dimensionless thermoelectric figure of merit of Bi/PbTe superlattices, using the carrier pocket engineering approach

Near-Term Milestones

- Studies on PbS/EuS superlattice will be further developed and compared to experiments, to be included in a first publication for this program
- Modeling of the PbS/Eu superlattice system will be developed and compared to experiments, to be included in the first publication for this program
- Completion of the theoretical model for the dimensionless thermoelectric figure of merit for the Bi/PbTe superlattice system using the carrier pocket engineering approach

Long-Term Milestones

- Develop theoretical models for the dimensionless thermoelectric figure of merit *ZT* for the generic family of group IV-VI compound semiconductor superlattices using the carrier pocket engineering approach, and apply this approach to specific experimental systems
- Develop a theoretical model for the dimensionless thermoelectric figure of merit *ZT* for the $Bi/Pb_{1-x}Eu_xTe$ superlattice system using the carrier pocket engineering approach, and apply the model to experimental results as they become available
- Characterize single layer, two layer, and superlattice samples of IV-VI compounds prepared by the Kharkov, Ukraine group with whom we collaborate or other groups, using TEM techniques
- Study the thermoelectric and transport properties of individual single layers, and single periods of AB and BA, where A and B are two constituents of a superlattice of interest, as a function of layer thickness and temperature, as samples become available
- Develop models to explain the effect of the barrier layers on the thermoelectric properties as a function of barrier thickness and species, and to compare the model calculations to experimental results as they become available
- Model the influence of the layer growth orientation on the thermoelectric parameters and to compare our model calculations to experimental results as they become available
- Model the effects of lattice misfit, island growth and quantum dot effects on the thermoelectric properties of IV-VI superlattices
- Analyze the temperature dependent conductivity, Hall effect and Seebeck coefficient measurements to determine the temperature dependent carrier mobility and to identify the relevant scattering mechanisms
- Develop models for the thermoelectric properties for superlattices with band inversion structures and compare model calculations with available experimental results

Demonstration Activity

Demonstrations of our achievements will be in the form of publications.

Performer: University of Maryland

Microfabrication Alliance for Innovative Cooling of Microelectronics (MAICOM)

PI: Professor Yogendra K. Joshi 301-405-5428

Other Team Members:

University of Maryland, Professor D. DeVoe, Dr. W. Nakayama
Sandia National Laboratories, Drs. P.M. Smith and C.V. Robino
ViA, Inc., Mr. Robert Palmquist
National Security Agency, Dr. W. Johnson, Ms. J. LaTondre, Mr. B. Pines
Hewlett-Packard Laboratories, Mr. C. Patel

Agent: NSWC Crane

Mr. Jeff Harms 812-854-2398

Project Goals

To develop, implement and deploy, innovative, on-demand, compact, flexible, robust and low cost cooling approaches for electronics at the chip, package and substrate levels, to handle ever increasing volumetric heat generation rates and reduce thermally induced stresses.

Approach

Two-phase thermosyphons with compact evaporators will be developed that employ microfabricated boiling enhancement structures of high thermal conductivity materials. Compact, single phase and two-phase forced fluid loops incorporating microfabricated heat exchangers will also be developed to achieve greater flexibility in system design. The second category of cooling devices utilizes capillary effects for liquid transport. Thin, flat, high performance heat spreader substrates using such microfabricated wick structures will be developed. The performance of these spreaders will be enhanced with the development of high aspect ratio micro-machined structures for efficient capillary transport of the coolant. Prototype cooling devices will be jointly fabricated by the University of Maryland, National Security Agency, and Sandia National Laboratory, and will be evaluated for implementation by ViA Inc., Hewlett Packard and National Security Agency on several test beds.

Accomplished Milestones

- Construct themosyphon using boiling enhancement structures in copper -- Jan. 2000
- Complete first heat pipe spreader incorporating high aspect ratio microstructures -- Jan. 2000
- Develop computational model to characterize thermal performance of single phase forced flow loops employing stacked micro-channels -- Dec. 1999
- Develop dynamic model of piezoelectric micropump and optimize geometry and piezoelectric layer thickness -- Feb. 2000
- Define test vehicles for demonstration of themosyphons and heat pipe spreaders -- Feb. 2000
- Develop conceptual design of the ViA Motion wearable computer and identify preliminary system heat dissipation requirements -- Jan. 2000

Near-Term Milestones

- Assess pump assisted thermosyphon performance for orientation independence
- Complete fabrication of initial micropump prototypes
- Assess theoretical micropump power efficiencies and redesign micropumps for increased power efficiencies
- Evaluate performance of commercial micropump from IMM (Germany)
- Assess thermosyphon reliability for extended operation
- Fabricate micro heat pipe spreader wick in silicon/silicon carbide
- Simulate thermosyphon performance computationally
- Validate thermal modeling capability for heat pipe spreaders
- Integrate and deliver a fully functional wearable computer system, called the ViA Motion, which uses the heat pipe spreader technology

Long-Term Milestones

- Develop and evaluate thermosyphon prototypes using boiling enhancement structures in diamond and silicon carbide
- Optimize piezoelectric micropumps for specific flow loop requirements
- Develop microfabricated single phase flow loops, incorporating stacked microchannel structures in high thermal conductivity materials and integrated micro pumps

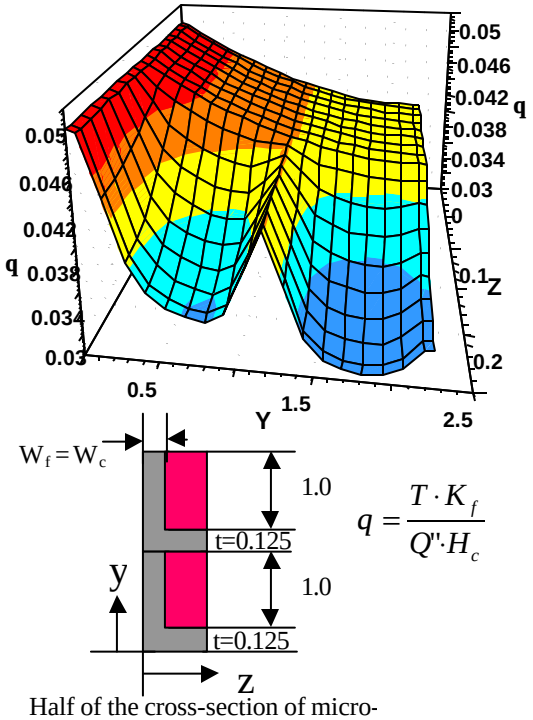
- Develop system level modeling of heat pipe spreaders and flow loops
- Demonstrate significantly higher thermal management capabilities in wearable and high performance desktop computing systems using compact liquid cooling schemes
- Assess reliability of thermal management schemes

Demonstration Activity

A demonstration vehicle will be developed to implement a compact thermosyphon in a high speed computing platform at HP.

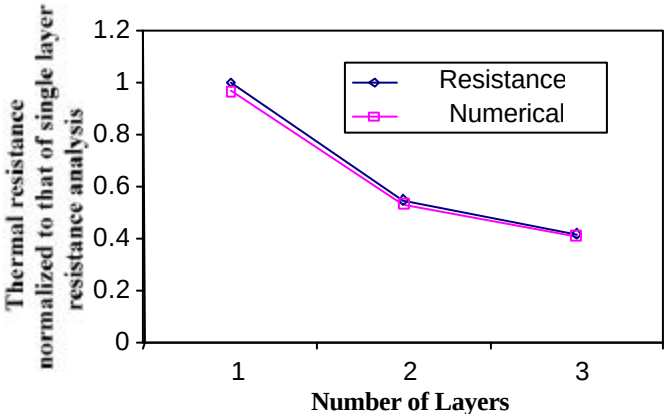
Thermosyphon and flow loop technologies will be demonstrated on a MCM test vehicle by NSA.

At the end of each year of this three year program, the team will demonstrate and deliver a fully functional wearable PC that uses the MAICOM heat dissipation technologies. ViA will include processor intensive applications, such as voice-to-voice language translation, as part of these demonstrations.



Half of the cross-section of micro-channel (Double layer)

Temperature profile computed for a two-layer stacked mircochannel.



The effect of number of layers in a stacked microchannel on thermal resistance. All computations are at a fixed pressure drop. Two types of analytical schemes are employed - a resistor network calculation and a three-dimensional fluid flow and heat transfer code.

Commercially available micropump from *Institute for Microtechnology* (Germany). Maximum mass flow rate is 350 µL/min and head of 2 bar. This will be used for evaluation of flow assisted thermosyphons

Mockup of Via Motion waist worn computer. Via Motion will use micro heat pipe heat spreader technology for thermal management.

Performer: University of North Carolina at Charlotte

Heat Removal by Inverse Nottingham Effect

PI: Professor Raphael Tsu (704) 547-2083

Other Team Members:

UNC-Charlotte, Dr. R. Greene
Sarnoff Corp., Dr. H. Busta
SUNY-Stony Brook, Dr. K.K. Likharev
NCSU, Drs. J. Cuomo and J. Hren

Agent: ARO

Dwight Woolard (919) 549-4297

Project Goals

The main goal of the project is to demonstrate the advantage of cutting the thermal link by pulling the hot electrons above the Fermi level of the semiconductor into the vacuum resulting in cooling the semiconductor. Due to the presence of a gap (vacuum), the voltage on the anode is much higher than between ohmic contacts. Therefore, a Pierce extraction electrode would be used to provide means for recovering the extra energy as practiced in traveling wave tubes. The primary goal is to realize cooling of the semiconductor via emission of hot electrons into the vacuum.

Approach

- Only electrons above the Fermi level are pulled out into the vacuum. This may be accomplished by surface inversion of a p-type semiconductor under the application of a high surface electric field. Under subcontract to SUNY, a method of using n-type has been studied.
- High field emission is achieved by either tip emitters, or, preferably by a double barrier resonant tunneling quantum well structure at the surface, to achieve higher and possibly more controllable field emission into the vacuum.

Accomplished Milestones

- Theoretical understanding of the items listed in the approach have been obtained.
- Resonant tunneling (RT) structures using p-GaAs/GaAlAs tunneling structure for emission into the vacuum have been measured by Sarnoff Corp. At present, no cooling has been observed because of the capping layer used to protect GaAlAs has too high work function, resulting in insufficient tunneling into the vacuum for achieving cooling.

Near-Term Milestones

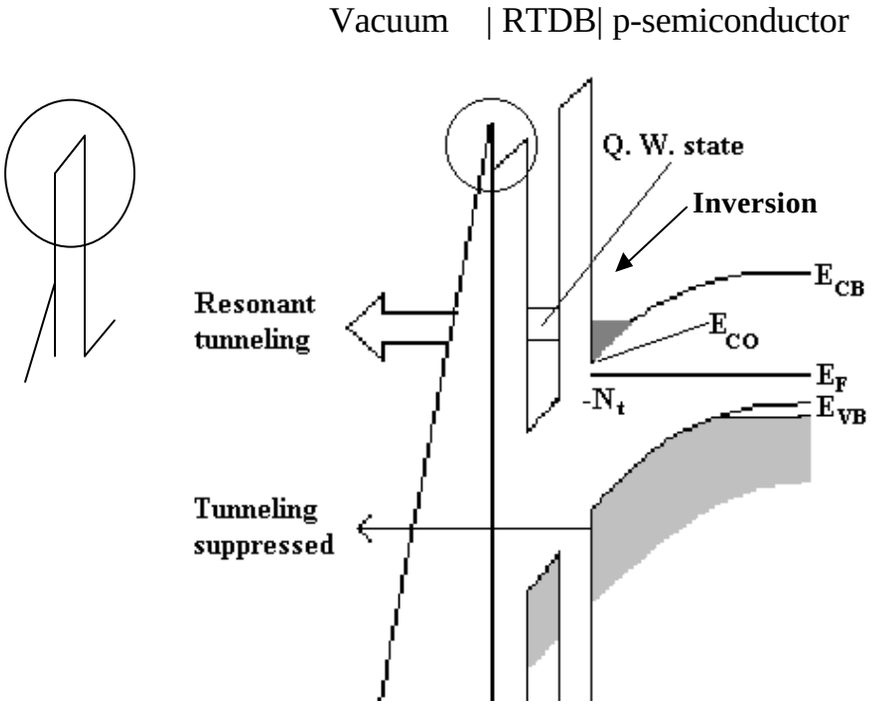
- We proceed to replace the GaAs/AlGaAs resonant tunneling system by GaN/AlGaN system which needs no capping protection. Besides the GaN system has a huge advantage of being NEA (negative electron affinity) for AlGaN, capable of much higher tunneling current into the vacuum.
- Hopefully GaN based test structures will show cooling.
- The RT based field emission should have wide applications in vacuum electronics.

Long-Term Milestones

- The emitter structure will be combined with the Pierce extraction system to achieve overall cooling. Comparison of the cooling rate with other thermoelectric coolers will be made.
- Microchannel heat removal will be combined to demonstrate cooling for ICs.
- Possibility of spot cooling will be considered. For example, cooling will be focussed onto an active transistor.

Demonstration Activity

Uniformity of field emission using RT structure will be demonstrated. Cooling power will be demonstrated with an actual IC circuit.



Band profile of p-doped inversion layer under high electric field with tunneling into the vacuum via a double barrier resonant tunneling structure. The circle indicates the vacuum level higher than the front barrier. The barrier width may be much reduced with NEA as shown at left for higher tunneling current into the vacuum. Also shown is trapping level at the interface, N_t, to be incorporated for increased replenishment of electrons pulled out into the vacuum.

Summary

- Cutting the thermal link with a vacuum should provide better cooling. RT replaces emitter tips for better emission uniformity and to avoid current crowding which results in extra heating.
- Inversion of p-type semiconductor is used for better control of electron emission above E_F.
- The front barrier ideally should be of NEA such as AlGaN for higher emission current.
- We failed with GaAs/GaAlAs system because the front barrier is too thick with protective capping. Our new effort is focussed on GaN/AlGaN system. Because of NEA for AlGaN resulting in a much thinner barrier at the vacuum side of the RTDB structure, emission into the vacuum should be much enhanced.
- High vacuum emission via RT should have wide applications in vacuum electronics.
- Eventually our scheme will be applied to silicon structure.

Performer: University of Utah

Integration of Thermoacoustic Cooling Devices with Microelectronic Circuits for Heat Removal

PI: Professor Orest G. Symko (801) 581-6132

Agent: Space and Naval Warfare Systems Center

Dr. Cynthia Hanson (619) 553-5242

Project Goals

The main goal is to integrate thermoacoustic cooling devices with microcircuits. The devices will be used for cooling electronic components and for pumping heat away from circuits. Since the devices operate in a resonant mode they will be scaled down in size by raising the operating frequency from 5 kHz to above 20 kHz. The demonstration that thermoacoustic devices can be microfabricated for integration with circuits will lead to an efficient approach for heat management in computers and electronics.

Approach

Combine on a chip piezoelectric driver, resonator, stack and heat exchangers thus forming a thermoacoustic device. Scale down size of device in steps leading to operation at frequencies above 20 kHz. Power density will be raised by operating at high pressures.

Accomplished Milestones

- Design of thermoacoustic device for circuit integration
- Evaluation of heat transfer problems within the device and with rest of circuit
- Evaluation of sound interference with circuit and environment

Near-Term Milestones

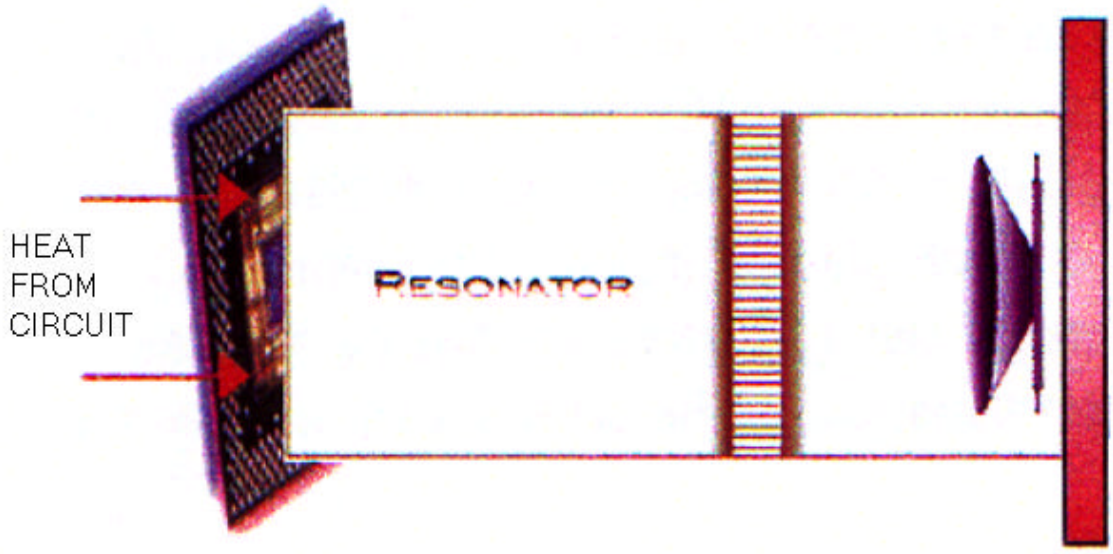
- Incorporate 5 kHz device with a circuit
- Characterize its performance as to heat transfer power, efficiency
- Use above results for miniaturization of devices

Long-Term Milestones

- Proof of concept that miniature thermoacoustic devices can be used for heat management on circuit
- Build chip-size thermoacoustic devices for integration with circuits
- Deliver a circuit module which contains a thermoacoustic cooling device for managing thermal problems on circuit
- Deliver a device which produces local cooling on circuit and a device which pumps heat away from components of circuits

Demonstration Activity

Develop a prototype device which shows how it removes heat from a circuit.



Thermoacoustic device for heat removal from circuit.

HERETIC Publications

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Leoni, N. and Amon, C. H., "Bayesian Surrogates for Integrating Numerical, Analytical and Experimental Data: Application to Inverse Heat Transfer in Wearable Computers," IEEE Transactions Comps., Pack. Technology, Vol. 23, No. 1, March 2000.

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Narumanchi, S., Amon, C. H. and Murthy, J., "Dielectric Jet Impingement Cooling of Electronic Chips," ASME Heat Transfer Conference 2000, Pittsburgh, PA, August 2000.

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D.-J. Yao, C.J. Kim, G. Chen, , J.-P Fleurial, and H. B. Lyon., "Spot Cooling Using Thermoelectric Microcoolers," The 18th International Conference on Thermoelectrics, Baltimore, MD, August 29-September 2, 1999.

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University of California, Los Angeles

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J. Wang and I. Catton, "Evaporation Heat Transfer in Thin Porous Media," Submitted to Journal of Heat Mass Transfer, 1999.

S. Jiang, and V. K. Dhir, "Heat Removal Using Phase Change Microdroplets." Accepted for the 34th ASME National Heat Transfer Conference, Pittsburgh, Pennsylvania, August 20 - 22, 2000.

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X. Fan, G. Zeng, E. Croke, G. Robinson, C. LaBounty, A. Shakouri, and J. E. Bowers, "n- and p-type SiGe/Si Superlattice Coolers," ITherm 2000 Conference Proceedings, Las Vegas, NV, May 2000.

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